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Low Power Square Root Carry Select Adder Using AVLS-TSPC-Based D Flip-Flop

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ABSTRACT

Speed, power, and area are the parameters to be considered while designing any integrated circuits including adder circuits. Low-power computation circuits play an important role in the very large-scale integration (VLSI) industry. Carry select adder (CSLA) is one of the fastest adders available and used to combat carry rippling. The square root of carry select adder (SCSLA) is a special case of CSLA. Since the SCSLA functions at high speed, it becomes vital to minimize the power dissipation and optimize the entire adder circuit. Adaptive voltage level at source (AVLS) is a technique used to minimize the power utilization of the circuit by decreasing the supply voltage. True-single phase clocking (TSPC) is used to design D flip-flop which reduces both the area and power. The proposed 16-bit adder architectures, one with AVLS normal TSPC-based D flip-flop and the other with AVLS modified TSPC D flip-flop has power reduction of 53.91% and 58.12% respectively, when compared with existing architectures in complementary metal-oxide-semiconductor (CMOS) 180 nm technology. Also, the proposed architectures, when implemented in CMOS 45 nm technology showed a power reduction of 82.75% and 82.93% respectively. The circuits are realized using Cadence Virtuoso and simulated using Cadence Spectre. Both the adders are power-efficient and operate at high speed.

***Index Terms*—**Adaptive voltage level at source (AVLS), carry select adder (CSLA), D flip-flop, low power, square root of carry select adder (SCLSA).

I. INTRODUCTION

Logic style and micro-architecture are the critical design features for any arithmetic circuit [1]. Arithmetic circuits are used to execute various calculation purposes such as addition, subtraction, multiplication, address calculation, media access control address (MAC) unit, etc. [2]. Low-power computation circuits play an important role in the VLSI industry. In processors, such as the digital signal processor, the essential modules are the adders. The MAC unit utilizes a full adder, which significantly affects the efficiency of the complete system. Multiplication is also an imperative arithmetic operation which is implemented using addition of partial products [3]. Hence, low-power adder becomes the need of the hour for achieving high-performing processors and systems.

The addition in the adders is limited by the propagation of the carry signal. Carry select adder (CSLA) is better than ripple carry adder (RCA) as it has less delay. Considering the carry propagation design for adders, an acceptable compromise can be achieved between cost and performance while using the carry select method [4]. Linear CSLA uses two rows of RCAs, one operating with carry_in = "0" and the other with carry_in = "1." As a result, two predetermined sets of sum and carry_out signals are obtained. The precise output is selected using the original carry_in. The square root carry select adder (SCLSA) is a variant of CSLA. The SCSLA design is an advancement over the standard (linear) CSLA in terms of power dissipated and operating speed [5]. Carry is propagated to successive blocks through multiplexers. Due to the inclusion of additional RCAs in SCSLA, it consumes more power as compared to RCA. Hence, it becomes necessary to reduce the power consumption of SCSLA to implement it in low-power applications.

The SCSLA can be made low power using true single-phase clock (TSPC)-based D flip-flops in place of RCAs. The TSPC-based D flip-flop is a dynamic CMOS-based flip-flop that aims at operating at an elevated speed. However, in an effort to further lower the consumption of power by SCSLA, the adaptive voltage level at source (AVLS) approach has been incorporated. Adaptive

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voltage level at source is a technique in which the power consumption is reduced by lowering the supply potential [6]. A sleep-control signal, often the clock signal, is used to regulate the operation of the AVLS circuit's transistors. It lowers the voltage across the gate source and drain, hence, lowering the leakage power. The AVLS circuit's output serves as the supply voltage for the SCSLA.

This study emphasizes on proposing a 16-bit SCSLA architectures that dissipates low power with less carry rippling delay. The proposed SCSLA uses AVLS logic with TSPC-based D flip-flops instead of RCAs. By incorporating AVLS and TSPC-based techniques in the proposed adder, the power and speed parameters are optimized respectively. Cadence Virtuoso is utilized to realize the proposed architecture, while the simulation is carried out on Cadence Spectre.

The paper is categorized into various sections. Frameworks, techniques, and realizations are reviewed in section II. Section III elucidates the CSLA and the AVLS technique. The implementation of the TSPC-based circuits and proposed architecture is explained in section IV. Section V analyses the simulation results and compares the proposed adders to the existing adder, with regard to power utilized and delay parameters. Section VI concludes the work and puts forth the future scope to it.

II. ASSOCIATED WORKS

The arithmetic, as well as logic units in microprocessors and microcontrollers, consists of a full adder which acts as the basic arithmetic circuit. Hence, the overall capability of circuits that consist of the full adder can be upgraded by improving the performance of the adder. Nigam and Singh [2] described a relative analysis of full adders consisting of 28T and 14T. The evaluation was done owing to the consumption of power, by altering the values of different parameters. It was remarked and proved that the 14T full adder consumes less power as compared to the 28T full adder. The implementation and simulation were done with Empyrean Aether employing 45 nm technology libraries.

The structure of the CSLA was modified to overcome power dissipation problems [4]. A TSPC-based D-FF was used to replace the carry input block. The suggested configuration was better with regard to power as well as area when compared to the standard and CSLA based on binary to excess-1 converter (BEC), with a power consumption of 7.951 mW for 16 bits.

Anirvinnan et al., [6] suggested a new technique for low-power application, by using D flip-flops with minimal power consumption. The realization of latches and flip-flops was achieved by this strategy of the TSPC circuit which lessened the skew issues in the clock. By adapting AVLS into the circuits based on TSPC, the target of low-power was also achieved. Adaptive voltage level at source was perceived to utilize lesser power when contrasted with that of adaptive voltage level at ground (AVLG). Therefore, it was then integrated with TSPC-based flip-flop. The TSPC circuit was designed using 10T. This methodology, without AVLS technology, was found to utilize 21.9 μW of power but with AVLS unification, it was then decreased to 9.304 μW providing an insignificant expansion in the area.

There is a need for a faster arithmetic processing unit due to rapid growth in the technology used these days, therefore, CSLA was considered. Linear CSLA was implemented in Naik and Rao [7] by replacing RCA with BEC. The authors also implemented a new approach of using D-latch so as to further reduce the power utilization. Results depicted the reduction of delay of CSLA architecture than the current models of BEC-based CSLA architecture and RCA-based architectures.

With efficient usage of area and reducing the power dissipation of the adder, the comprehensive performance of the processors can be enhanced. In the authors suggested the notion of using TSPC-based D-FF instead of using RCA and BEC in the conventional method. This prototype of 16-bit CSLA with normal TSPC-based D-FF used a fewer number of transistors as compared to RCA. Therefore, the power consumed was less compared to other circuits. The utilization of D-FF that triggers at the positive edge of the clock along with modified TSPC resulted in lesser power consumption and the product of power-delay was reduced [8].

Ponnusamy and Palaniappan [9] dealt with a new approach of implementing a negative edge-triggered D-FF instead of the regular D-FF with the 16-bit CSLA. This continuous switching of inputs directly impacted the outputs of the adder on the application of the enable signal. Their methodology was implemented in a partitioned Dadda multiplier using the microwind tool that worked at a faster pace. Results were marked with the length and width trade-off for power. The suggested CSLA architecture resulted in power consumption of 0.296 mW.

A new methodology known as TSPC flip-flop was used to compensate for the generation of leakage current at dynamic nodes of the transistor. Lee and Jang [10] proposed this technique for covering a vast range of operational frequencies in the CMOS processes. A gated inverter (GI) was used to build three feedback circuits which were then used to implement the suggested method of TSPC-based flip-flop. The suggested design was provided with a 1 V power supply and is operated at 2 GHz frequency. The results concluded that the recommended TSPC-based flip-flop shows zero error at low frequencies of 1 MHz.

The surveys of various models of D flip-flop depend on the TSPC rationale which permits to address the plan of D-FF with a more modest region and lower power utilization when contrasted with the master–slave arrangement-based D flip-flop [11]. The paper examined the execution of various TSPC-based D flip-flops and their correlation regarding power, delay, and transistors. In contrary with other flip-flops, it was seen that the 5T TSPC-based D-FF is better in execution with less utilization of power from the comparison result and analysis.

The optimization of power plays a crucial role in low-voltage and low-power applications. Gupta and Saxena [12] presented an architecture of a D-FF circuit utilizing AVL methods for low-power activity. The realization of this D-FF was done by making use of H-Spice with 130 nm technology. Results of simulation showed a reduction of power for the suggested cell adapting the AVL procedure. Elimination of unnecessary switching of the transistors, with respect to the clock signal in memory elements, found that the power dissipation can be reduced to a larger extent than the current methodology. The AVLS technique had a power consumption of 1.13 nW, whereas the AVLG technique

had a power consumption of 2.25 nW. Carry select adder proposed in [3] dissipates less power but occupies more area as adiabatic logic is incorporated in the design of the adder. There is a need to design a SCLSA which reduces power, delay, and area.

III. DESIGN THEORY OF ADDERS

Adders play a significant role as the basic arithmetic circuit in signal processors, microprocessors, and other applications. Hence, improving the performance of the adders portrays an imperative part in upgrading the overall circuit.

A. Ripple Carry Adder

The RCA is developed by cascading one-bit full adders to generate the sum as well as the carry signals. The sum and carry signals of the one-bit full adders are generated according to (1) and (2). The subsequent block produces a sum only after the preceding block is summed. The carry from the precedent blocks is passed onto the succeeding blocks for addition [13]. This configuration is efficient in terms of area, but the delay in propagation of carry signal from the previous blocks to the next results in the adder functioning at a slower speed. Since speed is a significant parameter in numerous applications, CSLA is preferred to overcome the delay of RCA:

$$S = A \oplus B \oplus Carry_{in} \tag{1}$$

$$Cout = A \cdot B + B \cdot Carry_{in} + Carry_{in} \cdot A \tag{2}$$

B. Carry Select Adder With Ripple Carry Adder

The linear n-bit CSLA is divided into m-blocks with equal bit-size. But there is a mismatched delay while obtaining the carry and sum signals. In SCSLA, the n-bit adder is divided into m-blocks with unequal bit-size. For a 16-bit adder, it is divided into five blocks with sizes of 2, 2, 3, 4, and 5-bits respectively from the rightmost block. Except for the rightmost block, all other blocks consist of two RCAs with each having carry_in "0" and "1,"respectively. The multiplexer (MUX) helps to overcome the mismatched delay present in linear CSLA [14]. The SCSLAperforms its operation very fast as compared to RCA because it does not wait for carry from the preceding block, rather performs the addition with the independent given carry signal. Hence, the sum and carry outputs are obtained at the MUX output. Fig. 1 shows a 16-bit SCSLA with RCA [4].

C. The Square Root Carry Select Adder With True-Single Phase Clocking-Based D Flip-Flop

The 16-bit SCSLA using the normal positive edge-triggered D-FF uses the RCA with the clock as carry_in for addition. When the clock becomes zero, the RCA performs the addition with carry_in = "0," and sends the result to the D-FF. During the positive edge of the clock, this result is accumulated in the D-FF. When the clock becomes high (or logic "1"), the RCA performs the addition with carry_in = "1," and sends it directly to the multiplexer, as the D-FF acts as a latch when the clock becomes high. The actual sum and carry are produced at the end of one complete clock cycle. An altered TSPC-based D-FF can be designed to decrease the utilization of power by removing one transistor from the normal TSPC-based D-FF and by making the required changes.

D. Adaptive Voltage Level

To achieve minimal dissipation of power by the circuit and to make it operate at low power, a technique called adaptive voltage level (AVL) is used. The AVL circuit is controlled by a sleep-control signal. The AVLG raises the potential of the ground, whereas the AVLS lowers the supply voltage potential, accordingly decreasing the dissipation of power by the entire circuit. Adaptive voltage level at source consists of a parallel connection of two NMOS transistors and one PMOS transistor. The two NMOS transistors are in turn concatenated in series. The clock signal is connected to the PMOS transistor node which acts as the input to the circuit. On the other hand, the supply is given to the input of NMOS transistors. The supplied clock acts as the sleep signal which controls the functioning of the AVLS circuit. Fig. 2 shows a principal AVLS circuit that is positioned in between the supply voltage and the SCSLA to lessen the potential of the supply node.

IV. DESIGN AND IMPLEMENTATION OF ADDER ARCHITECTURES

Cadence Virtuoso is used to implement all the circuits using both 180 nm and 45 nm technologies. Cadence Spectre is used to carry out the simulation of the frameworks. The SCSLA can be modified by implementing a D flip-flop instead of the second RCA in each block, with a

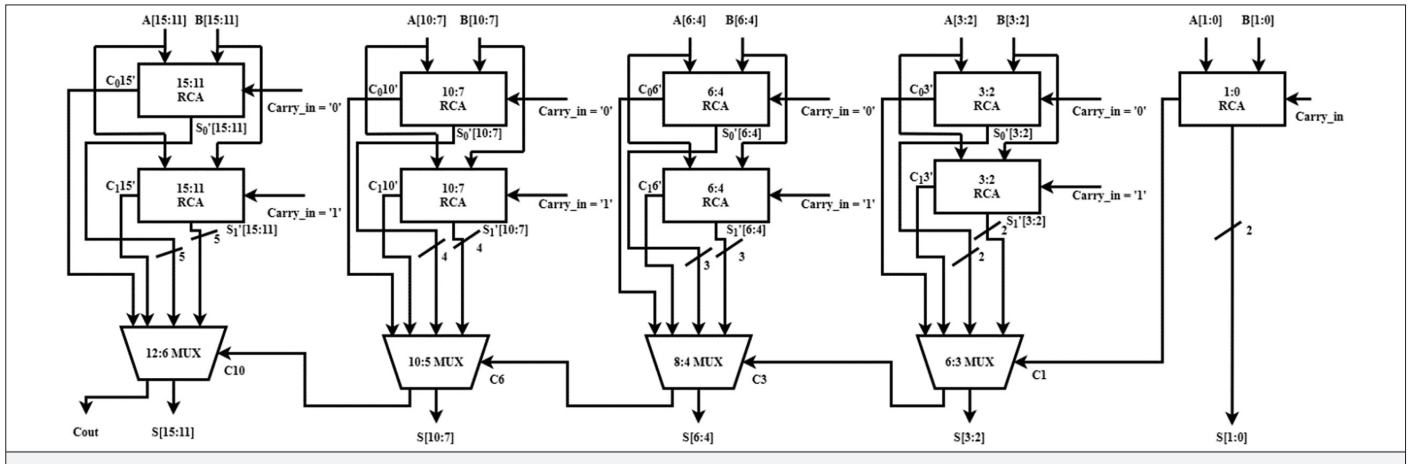

Fig. 1. Sixteen-bit square root carry select adder (SCSLA)with ripple carry adder (RCA).

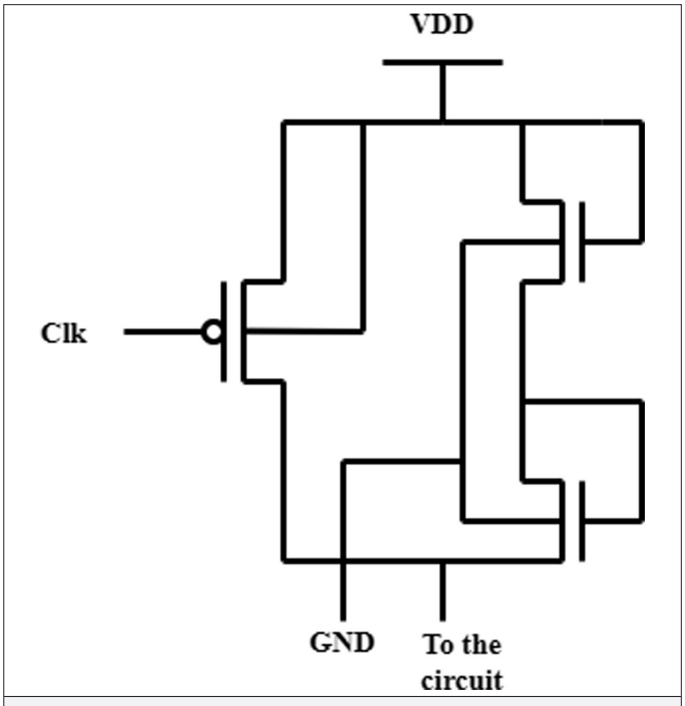

Fig. 2. Principle adaptive voltage level at source (AVLS) circuit.

motive to decrease the utilization of power along with the delay of the SCSLA. The D-FF can be realized to work at a faster rate by incorporating TSPC to the D-FF. True-single phase clocking allows the true phase of the clock and does not take the complement of it. The SCSLA with TSPC-based D-FF is efficient with reference to power, area, and delay.

The normal TSPC-based D flip-flop is implemented using 11 transistors. Only a single clock is seen in TSPC which is never inverted. The clock signal is given to both NMOS and PMOS transistors. The output is continuously affected by the switching of inputs with variation in the clock.

A TSPC clock minimizes the overall power consumption of the circuit as it requires fewer transistors, and thereby increases the speed of the circuit. True-single phase clocking acts as master and slave circuits.

The SCSLA can be made power and speed efficient by implementing D-FF rather than the RCA in the second row. Fig. 3 displays the realization of a normal TSPC-based D flip-flop (11 T). The remodeled TSPC-based D-FF can be implemented by removing one transistor from the normal TSPC-based D flip-flop [4]. As the remodeled TSPC-based D-FF can be realized using 10 transistors, it dissipates less power in contrast with the normal TSPC-based D-FF. Fig. 4 shows the implementation of the modified TSPC-based D-FF.

Table I lists the power and delay values of the full adders. The TSPC-based D flip-flop consumes less power compared to the one-bit full adder. Hence, the normal and modified TSPC-based D flip-flop is preferred over RCA in SCSLA. Keeping in mind the goal to further decrease the power utilization of the normal and modified TSPC-based D flip-flop, the AVLS technique can be implemented. Since the D-FF is a sequential segment and makes use of a clock signal for its functioning, the same can be used as the control signal for the AVLS circuit. Fig. 5 shows the realization of AVLS normal TSPC-based D-FF.

In the AVLS circuit, the NMOS transistors are continuously in the ON state, as they are forward biased. The PMOS transistor has the clock signal as the input and hence toggles from one state to the other. As a result, the minimal discharge current flows through the PMOS of AVLS, thereby reducing the utilization of power by the circuit. Fig. 6 shows the realization of AVLS modified TSPC-based D-FF. Table II displays the power and delay results of AVLS normal and modified TSPC-based D flip-flop when realized using 45 nm technology libraries. It is evident that these architectures consume less power compared to the values listed in Table I.

Two designs have been proposed as a part of the proposed architecture. The proposed-1 design has AVLS normal TSPC-based D flip-flop

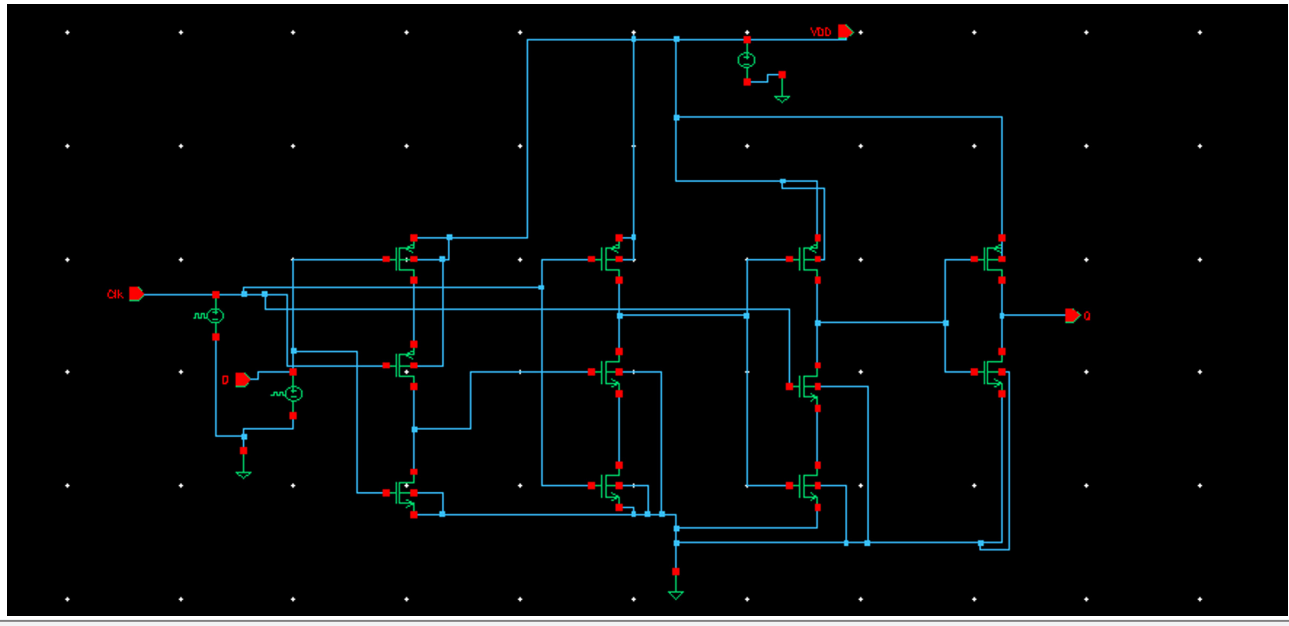

Fig. 3. Normal true-single phase clocking (TSPC)-based D flip-flop.

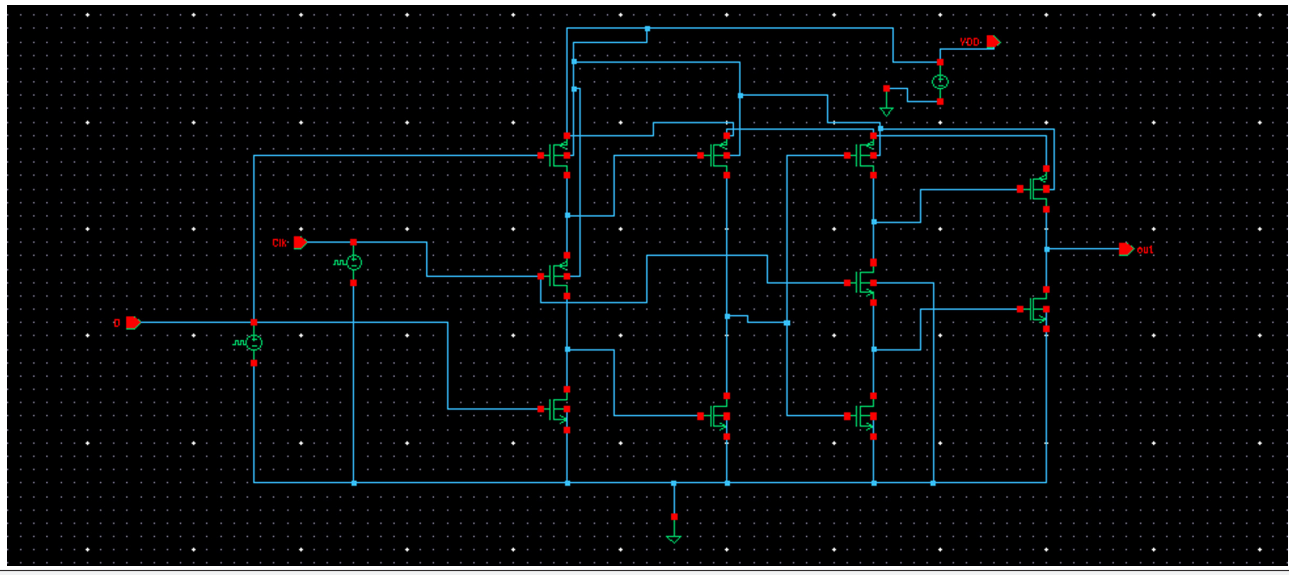

Fig. 4. Modified TSPC-based D flip-flop.

TABLE I. POWER AND DELAY ANALYSIS OF 1-BIT FULL ADDER, NORMAL, AND MODIFIED TRUE-SINGLE PHASE CLOCKING-BASED D FLIP-FLOP IN 45 NM TECHNOLOGY

Architecture	Transistor Count	Power (μW)	Delay (ps)
1-bit full adder	28	10.28	23.82
Normal TSPC-based D flip-flop	11	1.932	13.77
Modified TSPC-based D flip-flop	10	1.849	13.96

TSPC, true-single phase clocking.

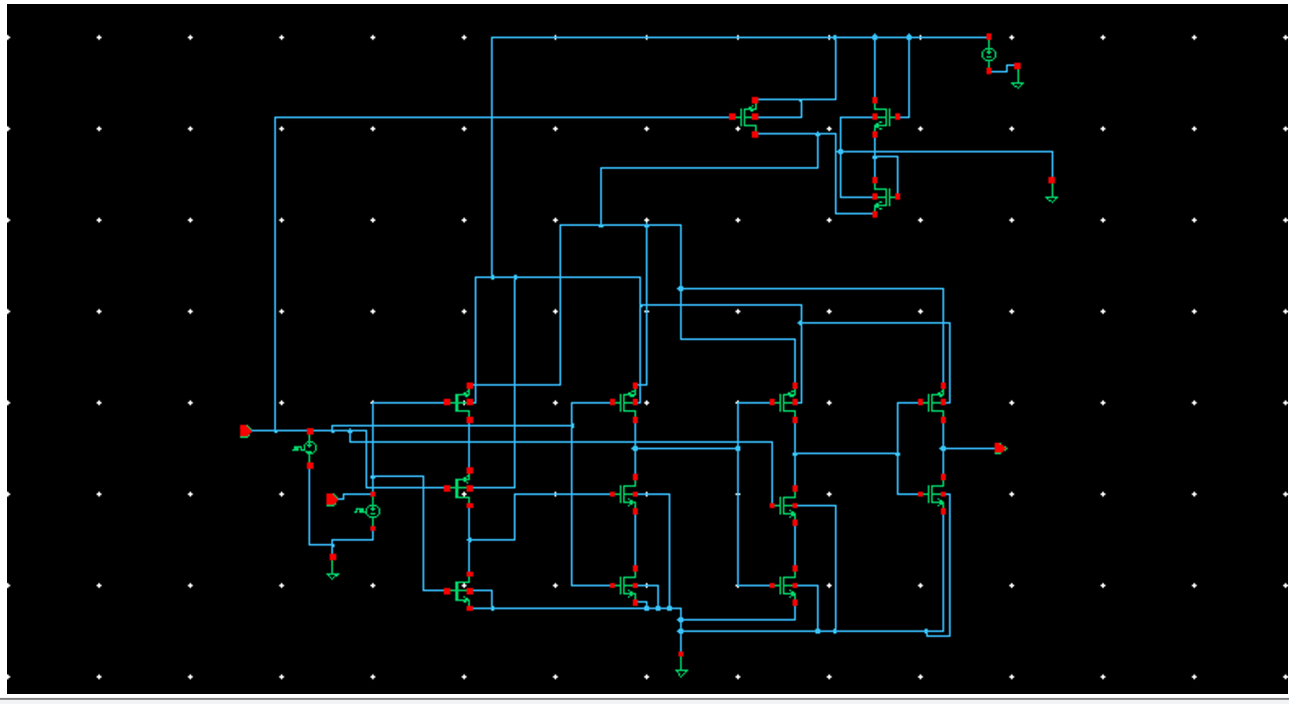

Fig. 5. Adaptive voltage level at source normal TSPC-based D flip-flop.

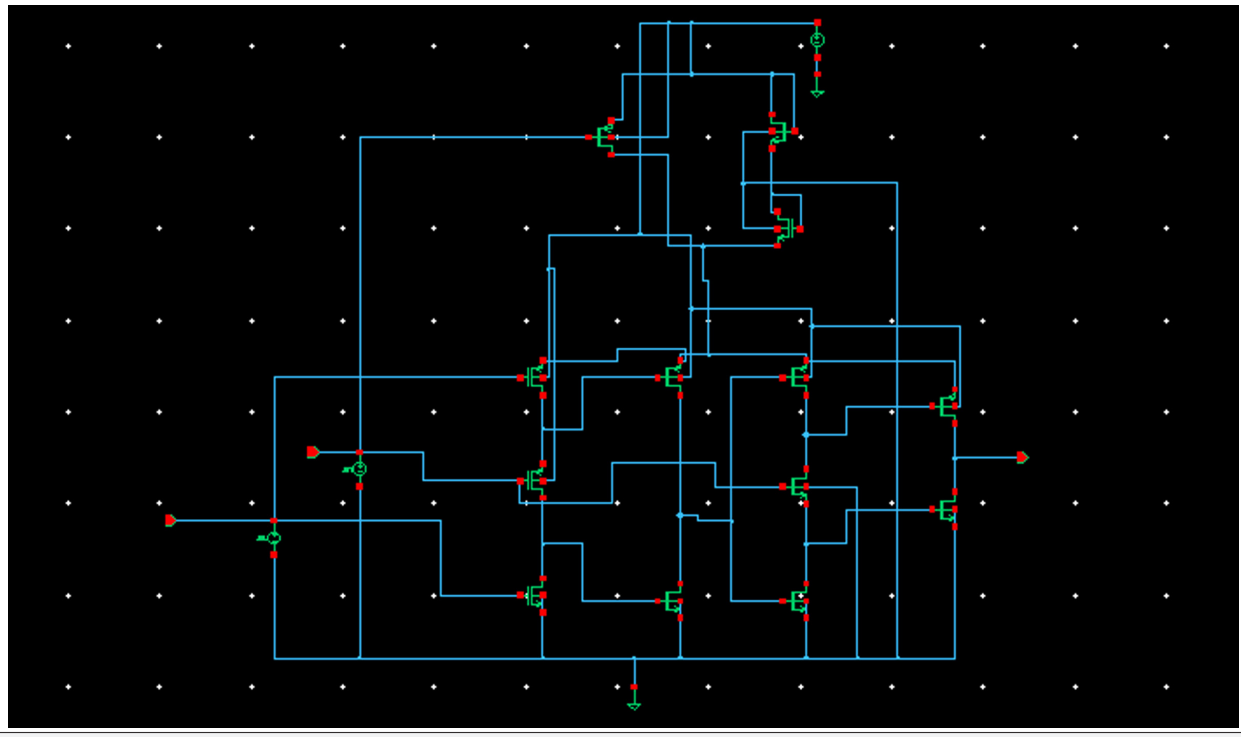

Fig. 6. Adaptive voltage level at source modified TSPC D flip-flop.

TABLE II. POWER AND DELAY ANALYSIS OF AVL NORMAL AND MODIFIED TRUE-SINGLE PHASE CLOCKING-BASED D FLIP-FLOP IN 45 NM TECHNOLOGY

Architecture	Transistor Count	Power (μW)	Delay (ps)
AVLS normal TSPC-based D flip-flop	14	1.614	14.98
AVLS modified TSPC-based D flip-flop	13	1.652	13.98

AVLS, adaptive voltage level at source; TSPC, true-single phase clocking.

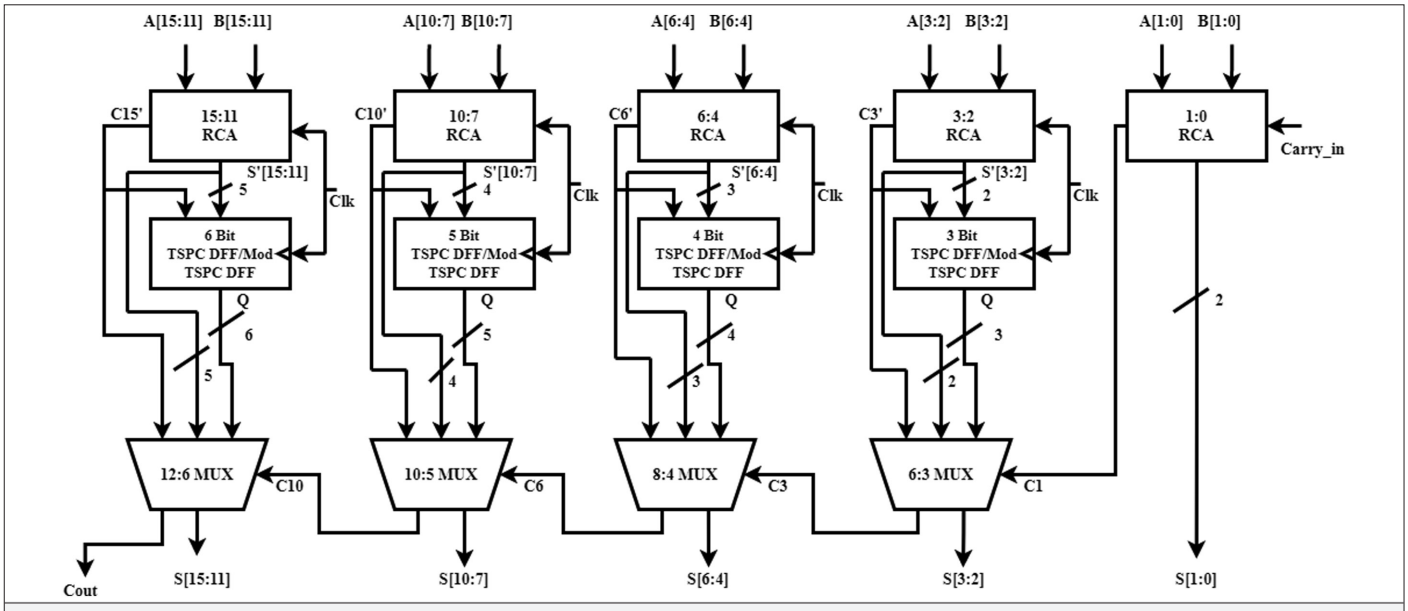

Fig. 7. Proposed 16-bit SCSLA with AVLS-TSPC-based D flip-flop.

(Fig. 5) and the proposed-2 design has AVLS modified TSPC-based D flip-flop (Fig. 6). These flip-flops are used instead of RCA in the second row of each block in the 16-bit SCSLA. Fig. 7 shows the proposed-1 and proposed-2 designs of 16-bit SCSLA with normal/modified TSPC-based D flip-flop. The AVLS circuit is placed between the supply voltage and the 16-bit SCSLA adder, with a clock signal as the input to the AVLS circuit.

The clock signal is common to both AVLS and 16-bit CSLA circuits. Due to this, the leakage flow of the PMOS transistor is reduced, thereby minimizing the dissipation of power by the entire 16-bit CSLA. When the clock is zero, the addition is performed by the RCA in the first row and the result is passed onto the D-FF. During the positive edge of the clock, the D flip-flop is triggered and hence, it stores the result. When the clock becomes high, the RCA performs the addition and the result is transferred directly to the multiplexer. The D-FF continues to hold the previous result, as it acts as a latch when the clock is high. At the end of one complete clock cycle, the actual sum and carry are obtained at the multiplexer output with the select line as carryout of the previous block.

V. RESULTS AND DISCUSSION

The existing architectures and proposed architecture are implemented in 180 nm technology as well as 45 nm technology using the Cadence virtuoso tool. The simulation of all the architectures is executed at 100 MHz operating frequency using Cadence Spectre. For illustration, various inputs have been assessed and the respective results are set out in Table III.

The AVLS normal TSPC-based D flip-flop can further be implemented with 16-bit SCSLA to obtain power and delay efficient adder. The AVLS technique can also be applied to the altered TSPC-based D-FF. The amount of power dissipated by the altered TSPC-based D-FF is reduced considerably on the implementation of AVLS logic. In 180 nm technology, the AVLS logic is applied only to the normal and modified TSPC-based D flip-flop, whereas in 45 nm technology, it is applied to the whole circuit, to obtain the desired low power adder.

Fig. 8 shows the output waveform of the proposed 16-bit SCSLA with AVLS normal and modified TSPC-based D-FF.

The proposed 16-bit adders are analyzed with respect to power and delay in both 180 nm and 45 nm technologies. The proposed SCSLA is implemented in CMOS 180 nm technology and is compared w.r.t. adders in [1] and [8]. The proposed SCSLA is also implemented in CMOS 45 nm technology to analyse the power and delay in lower technology nodes. Table IV shows the comparison of power and delay values of existing and proposed 16-bit adders in 180 nm technology. The addition using 16-bit RCA is slower due to the cascading of one-bit full adders. To reduce the delay of RCA, 16-bit SCSLA with RCA is implemented. The existing 16-bit RCA [1] had a power consumption of 1.107 mW. The existing 16-bit SCSLA with RCA in [8] had a power consumption of around 2.435 mW which is greater than the power consumption of 16-bit RCA. The RCAs are replaced by normal TSPC (proposed-1) and modified TSPC (proposed-2)-based D flip-flops, reducing the power consumption and delay of the SCSLA. The SCSLA with TSPC-based D flip-flop in [8] had a power consumption of around 1.588 mW, which is lesser than the 16-bit SCSLA with RCA. Also the architectures in [15] were remodeled and simulated using Cadence virtuoso.

The SCSLA with modified TSPC-based D flip-flop has a power consumption of 1.564 mW, due to the decrease in the number of transistors that constitute the D flip-flop. Furthermore, the power consumption of 16-bit SCSLA with normal and modified TSPC-based D flip-flop is reduced by implementing AVLS logic to the adders. The proposed 16-bit SCSLA with AVLS normal TSPC-based D-FF and AVLS modified TSPC-based D-FF has a power consumption of 731.8 μW and 654.9 μW, respectively. A power reduction of 53.91% and 58.12% can be observed when AVLS normal TSPC-based D-FF and AVLS modified TSPC-based D-FF are used, respectively, with 16-bit SCSLA. The same trend of power reduction is observed when the adders are implemented in 45 nm technology. But, the magnitude of power consumption is notably small in 45 nm technology.

TABLE III. SIMULATION PARAMETERS FOR 16-BIT ADDERS

A	B	Carry_in	Cout	Sum
1111 1110 0001 0100	0100 1001 1110 1111	1	1	0100 1000 0000 0100
0001 1011 1111 1111	1111 0110 1011 0011	1	1	0001 0010 1011 0011
1111 0111 1101 1001	1001 1111 0101 1110	1	1	1001 0111 0011 1000
0001 1010 1110 1011	1011 0110 0011 0011	0	0	1101 0001 0001 1110
1110 1101 1101 1101	1101 1111 1111 1101	0	1	1100 1101 1101 1010
0001 0011 0111 1110	1110 0010 1001 0010	1	0	1111 0110 0001 0001
1111 1110 1101 1001	1001 1111 0111 1111	1	1	1001 1110 0101 1001
0001 1011 1010 0011	0011 0100 0011 0011	1	0	0100 1111 1101 0111
1111 0111 1101 1101	1101 1111 1100 1110	0	1	1101 0111 1010 1011
0000 1000 1111 1111	1111 0110 1011 0001	0	0	1111 1111 1011 0000

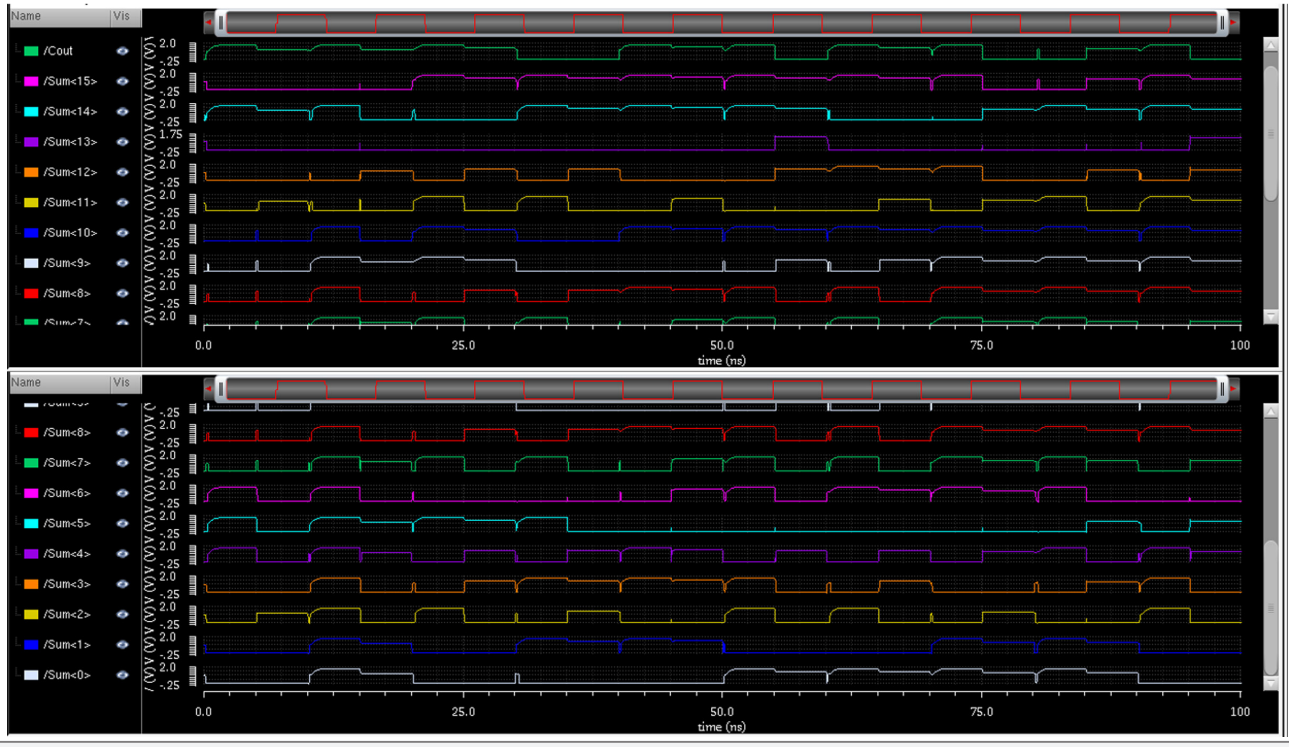

Fig. 8. Output waveform of 16-bit SCSLA with AVLS normal/modified TSPC-based D flip-flop.

TABLE IV. COMPARISON OF EXISTING AND PROPOSED 16-BIT ADDERS IN 180 NM TECHNOLOGY

16-Bit Adder Architectures	Power (μW)	Delay (ps)
RCA [1]	1107.37	1062.56
SCSLA with RCA [8]	2435.43	844.2
SCSLA with normal TSPC-based D flip-flop [8]	1588.54	696.2
SCSLA with D flip-flop [16]	1595.28	698.7
Proposed-1 SCSLA	731.8	635.18
Proposed-2 SCSLA	654.9	651.29

SCSLA, square root carry select adder; TSPC, true-single phase clocking; RCA, ripple carry adder.

Table V shows the power and delay results of 16-bit adders in 45 nm technology. In 45 nm technology, the proposed 16-bit SCSLA with AVLS normal TSPC-based D-FF has a power consumption of 26.7 μW, whereas the 16-bit SCSLA with AVLS modified TSPC-based D-FF has a power consumption of 26.42 μW. The proposed-1 design is better in terms of delay and the proposed-2 design is better in terms of power compared to the architectures in [16] which were remodeled and simulated using Cadence Virtuoso. Both the proposed designs have marginal variations among themselves with respect to power and delay. Hence there is a trade-off between both the proposed architectures. Based on the power or delay constraints, the proposed-1 and proposed-2 architectures can be selected respectively.

TABLE V. COMPARISON OF EXISTING AND PROPOSED 16-BIT ADDERS IN 45 NM TECHNOLOGY

16-Bit Adder Architectures	Power (μW)	Delay (ps)
RCA	135.9	194.36
SCSLA with RCA [15]	363.1	152.77
SCSLA with normal TSPC-based D flip-flop	154.8	89.6096
Proposed-1 SCSLA	26.7	58.59
Proposed-2 SCSLA	26.42	59.89

SCSLA, square root carry select adder; TSPC, true-single phase clocking; RCA, ripple carry adder.

A power reduction of 82.75% and 82.93% can be observed while using 45 nm technology libraries when the proposed adders are compared with the prevalent architectures. The prevalent architectures are implemented separately using 45 nm technology libraries and their simulation results are utilized for comparison.

VI. CONCLUSION AND FUTURE SCOPE

The speed of the adders is dependent on the carry propagation mechanism. In order to bring down dissipation of power, and improve the rate of addition, various 16-bit adders are analyzed. All the architectures are analyzed at 100 MHz operating frequency. The 16-bit SCSLA with RCA has less delay but consumes more power as compared to 16-bit RCA. To reduce the power consumption, the

RCA in SCSLA is replaced with a D flip-flop, which yields less power as well as less delay. Modified TSPC-based D flip-flop is used to get comparatively less delay and power than 16-bit SCSLA with normal TSPC-based D flip-flop. The AVLS technique is used to further reduce the power by a great margin i.e., 58.12% in 180 nm technology and 82.75% in 45 nm technology, thus yielding low power 16-bit SCSLA. It can be concluded that the 16-bit SCSLA with AVLS normal and modified TSPC-based D flip-flop consumes the least power among all other adders when implemented in 45 nm technology. The adders can be further extended as future work, for 32-bit, 64-bit, and 128-bit, and can be implemented in partitioned Dadda multipliers and other complex architectures, which play an important role in DSP applications.

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