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CURRENT-MODE BASEBAND DESIGN FOR INTEGRATED RF RECEIVERS

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ABSTRACT

In this study, in order to inherit the known advantages of the current-mode (CM) operation, a current-mode receiver baseband architecture is proposed for integrated RF receivers. The baseband circuitry is composed of a filter, a variable gain amplifier (VGA), and an analog-to-digital converter (ADC). However, ADC is not in the scope of our study. In the proposed architecture, the voltage-to-current conversion is performed during lowpass filtering in the first stage, where some variable gain is also provided. Thus, lowpass filter and variable gain amplifier is merged in the same stage. The following stage is a lowpass biquad that performs further filtering of the undesired signals. The simulation results show that the proposed architecture is suitable for low-voltage, low-power applications.

Keywords: *Active filters, current-mode circuits, variable gain amplifiers*

1. INTRODUCTION

The advances in very large scale integration (VLSI) technology makes it possible to pack large numbers of digital circuits in a given silicon area and therefore, operation at low supply voltages becomes essential in order to reduce the power consumption. On the other hand, with the analog and digital circuits on the same chip, the reduced voltage supply levels result in reduced dynamic range for the analog part [1]. In order to overcome this problem, the signal representation must be changed to current instead of voltage. Because, the low internal impedance levels generally related with the current-mode circuits yield reduced voltage swings and the signal range is no more directly restricted by the supply voltage [2,3]. Because the output signal of a MOS transistor is current in both common-source and common-gate amplifier configurations, MOS transistors are more suitable for current processing [4]. Thus, current-mode (CM) signal processing yields simpler circuit realizations and because of the low impedance nodes they are almost free of slew-rate limitations, which makes them suitable for high-speed applications [5,6].

In this study, a new block diagram is proposed in order to benefit the known advantages of CM operation at the baseband stage of the integrated RF receivers. The first stage in this architecture converts the voltage signal at the output of the RF mixer to current signal and also performs lowpass filtering. This voltage-to-current (transadmittance) lowpass filter (LPF) also

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provides variable gain. Thus CM VGA, which forms the second block in the proposed architecture, is merged with the transadmittance LPF. That means, the transadmittance LPF and the CM VGA are implemented as one block. The third block of the proposed architecture is a CM lowpass biquad and added for further filtering purposes. As a result, partial channel selection with a fourth order LPF is implemented in the proposed architecture.

2. BASEBAND ACTIVE FILTER

The proposed CM receiver baseband architecture is illustrated in Figure 1.

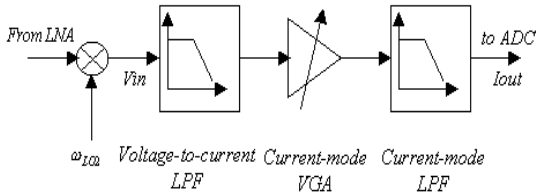

Figure 1. The block diagram of the proposed baseband architecture.

In this architecture single amplifier biquads, such as Sallen-Key filters, are used for active filter realizations, because of their compact implementation on silicon and low power consumptions.

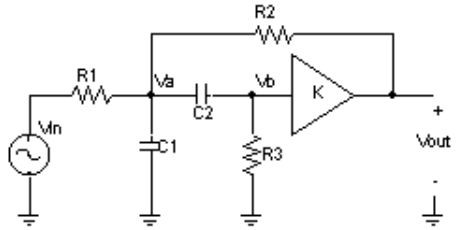

Figure 2. Conventional voltage-mode Sallen-Key BPF.

In the conventional voltage-mode Sallen-Key bandpass filter (BPF) shown in Figure 2, if the amplifier has a unity gain, then the current flowing through the feedback resistor R_2 has a lowpass characteristic and this current is also the output current of the voltage buffer when the circuit is not loaded. This idea can easily be implemented using a second-generation current conveyor (CCII) as the active element. The circuit symbol and its terminal relationship matrix of CCII are given in Figure 3.

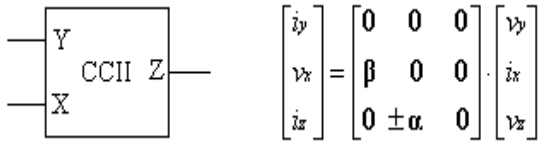

Figure 3. The symbol and terminal relationship matrix of CCII.

In the terminal relations matrix of CCII, β is the voltage gain between y-x and α is the current transfer ratio between z-x terminals. In some applications the voltage gain β and current transfer ratio α are equal to unity. In this case, a voltage tracking error ε_V is defined as the deviation of x terminal voltage from the y terminal voltage and a current tracking error ε_I is defined as the deviation of z terminal current from x terminal current. According to the sign of current transfer ratio α the CCII is called to be either positive or negative [7].

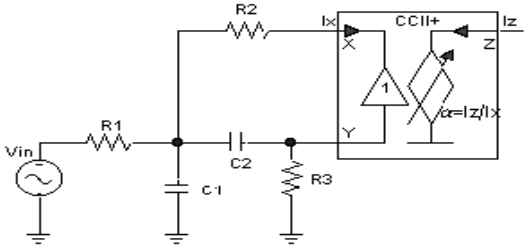

Figure 4. Transadmittance lowpass biquad

In the circuit given in Figure 4, the y-x unity gain cell is a voltage buffer and the current flowing through R_2 is transferred to z terminal by the help of the x-z unity current gain cell. Thus a transadmittance LPF with high output impedance is obtained, which makes it suitable for cascade connections in CM.

The transfer function of this circuit for β=1 is given in equation (1). It is obvious from equation (1) that the current transfer ratio α only appears in the numerator polynomial of the transfer function. Therefore, some variable gain may also be provided by properly changing α without spoiling the lowpass characteristic. In the proposed baseband architecture a decibel linear variable gain is obtained by changing α.

$$\frac{I_{out}(s)}{V_{in}(s)} = \frac{\dfrac{\alpha}{R_1R_2R_3C_1C_2}}{s^2 + s\cdot\left[\dfrac{1}{R_3}\left(\dfrac{1}{C_1}+\dfrac{1}{C_2}\right)+\dfrac{1}{R_1C_1}\right]+\dfrac{1}{R_3C_1C_2}\left(\dfrac{1}{R_1}+\dfrac{1}{R_2}\right)} \quad (1)$$

The natural frequency (ω_0), the quality factor (Q) and the DC transconductance (H_0) of this circuit are given in equations (2), (3) and (4), respectively.

$$\omega_0 = \sqrt{\frac{1}{R_3C_1C_2}\left(\frac{1}{R_1}+\frac{1}{R_2}\right)} \quad (2)$$

$$\frac{1}{Q} = \left[\frac{1}{R_3}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)+\frac{1}{R_1C_1}\right]\cdot\sqrt{\frac{R_1R_3C_1C_2}{1+R_1/R_2}} \quad (3)$$

$$Ho = \frac{\alpha}{R_1+R_2} \quad (4)$$

From equation (4), it is clear that if linear poly-silicon resistors are used for R_1 and R_2 resistors, then a highly linear voltage-to-current conversion can be implemented.

Additionally, the passive sensitivities of the circuit are exactly the same as the conventional voltage-mode Sallen-Key BPF except the sensitivities with respect to DC transconductance are specific and are as given in equations (5) and (6).

$$S_{R_3}^{H_0} = S_{C_1}^{H_0} = S_{C_2}^{H_0} = 0 \text{ and } S_{\alpha}^{H_0} = 1 \quad (5)$$

$$S_{R_1}^{H_0} = -\frac{1}{1+R_2/R_1} \text{ and } S_{R_2}^{H_0} = -\frac{1}{1+R_1/R_2} \quad (6)$$

Current-mode lowpass biquad that forms the second stage of the baseband active filter is shown in Figure 5 [8]. The order of the baseband active filter can be increased as desired by cascading appropriate number of this current-mode lowpass biquad The current transfer function of this circuit, for α=1 and β=1, is given in equation (7). The equations related to natural frequency (ω_0) and quality factor (Q) of this circuit are as given in (8) and (9), respectively.

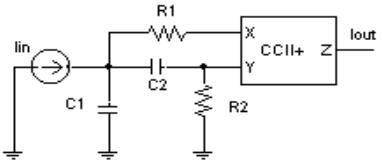

Figure 5. Cascadable current-mode lowpass biquad.

$$\frac{I_{out}(s)}{I_{in}(s)} = \frac{\dfrac{1}{R_1R_2C_1C_2}}{s^2+\left[\dfrac{1}{R_2}\cdot\left(\dfrac{1}{C_1}+\dfrac{1}{C_2}\right)\right]\cdot s+\dfrac{1}{R_1R_2C_1C_2}} \quad (7)$$

$$\omega_0 = \frac{1}{\sqrt{R_1R_2C_1C_2}} \quad (8)$$

$$Q = \sqrt{\frac{R_2}{R_1}\cdot\frac{C_2}{C_1}}\cdot\frac{1}{1+\dfrac{C_2}{C_1}} \quad (9)$$

From Figure 5 it is seen that this circuit is also cascadable for current-mode operations. The passive element sensitivities of this circuit are given in equations (10) and (11).

$$S_{R_1}^{\omega_0} = S_{R_2}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = S_{R_1}^{Q} = -S_{R_2}^{Q} = -\frac{1}{2} \quad (10)$$

$$S_{C_1}^{Q} = -S_{C_2}^{Q} = \frac{1}{2}\cdot\frac{C_2-C_1}{C_1+C_2} \quad (11)$$

If the equal-valued capacitors are chosen for this circuit, it is clear from equation (11) that the sensitivity of the quality factor with respect to capacitances will be equal to zero. In this case, the passive element sensitivities of the circuit will be really good.

The filter circuits in Figure 4 and Figure 5 are designed for the Digital Enhanced Cordless Telecommunications (DECT) system with 700kHz corner frequency and the element values are tabulated in Table1.

Table-1. The passive element values of the filters shown in Figure 4 and Figure 5 for DECT system.

	Figure 4	Figure 5
R1	16.11kΩ	3.21kΩ
R2	2.46kΩ	16.38kΩ
R3	31.95kΩ	N/A
C1	51.825pF	34.55pF
C2	17.275pF	34.55pF

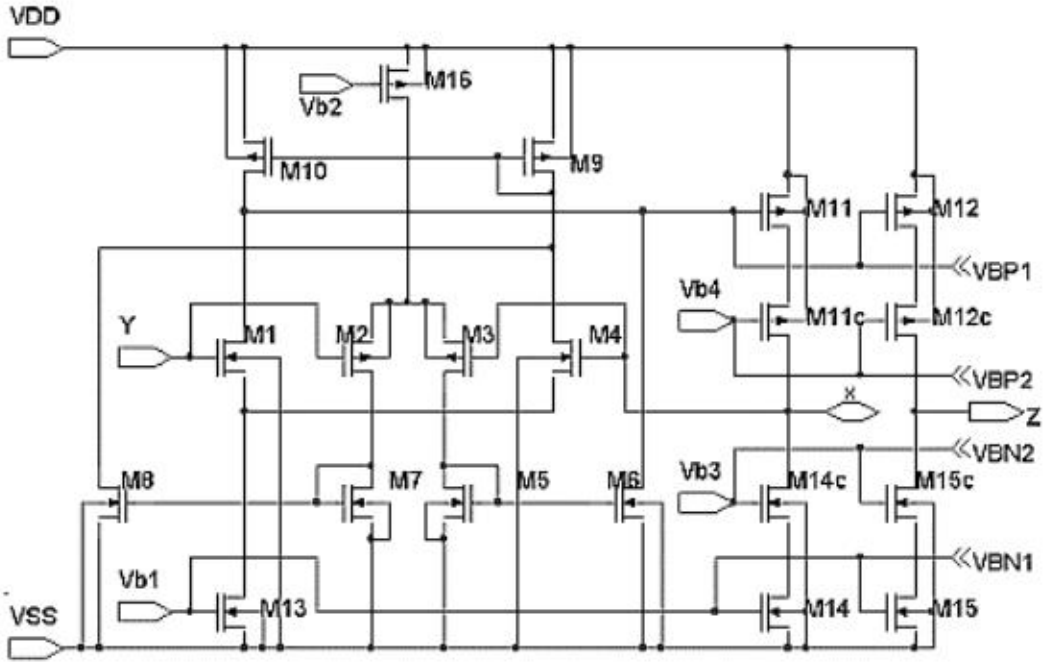

Figure 6. Class-A CCII used in filter configurations of Section 2.

3. VARIABLE GAIN AMPLIFIER

A variable gain amplifier is the core element of an automatic gain control (AGC) loop, which is used in mixed analog-digital system integrated circuits (ICs) to maximize the dynamic range of the overall system [9-13]. In wireless systems, due to receiver portability, the received signal power varies according to the distance to transmitter. The function of AGC in RF receivers is to adjust the gain of receive path in order to obtain constant signal level at baseband circuits [9,10].

The CCII circuit used in the filter configurations used in Section-2 is given in Figure-6 [13]. The main idea of providing decibel-linear variable gain depends on the formulation given in equation (12) [13].

$$I_{out} = I_{in} \cdot (1+1+2+2^2+2^3+\cdots 2^{n-1}) = I_{in} \cdot 2^n \tag{12}$$

According to this equation, in the decibel scale the current gain is $n \cdot 20\log 2 \cong n \cdot 6dB$. The simplicity of the current summation in the current-mode circuits gives us the opportunity to implement the equation given in (12) by modifying the output stage of the current conveyor in Figure-6 as in Figure-7. Here, a gain control mentality is aimed depending on increasing the current transfer ratio of the cascode circuits at the output by adding parallel transistors to the output. Therefore, with a very simple method the output stage of the current conveyor in the transadmittance filter also provides variable gain

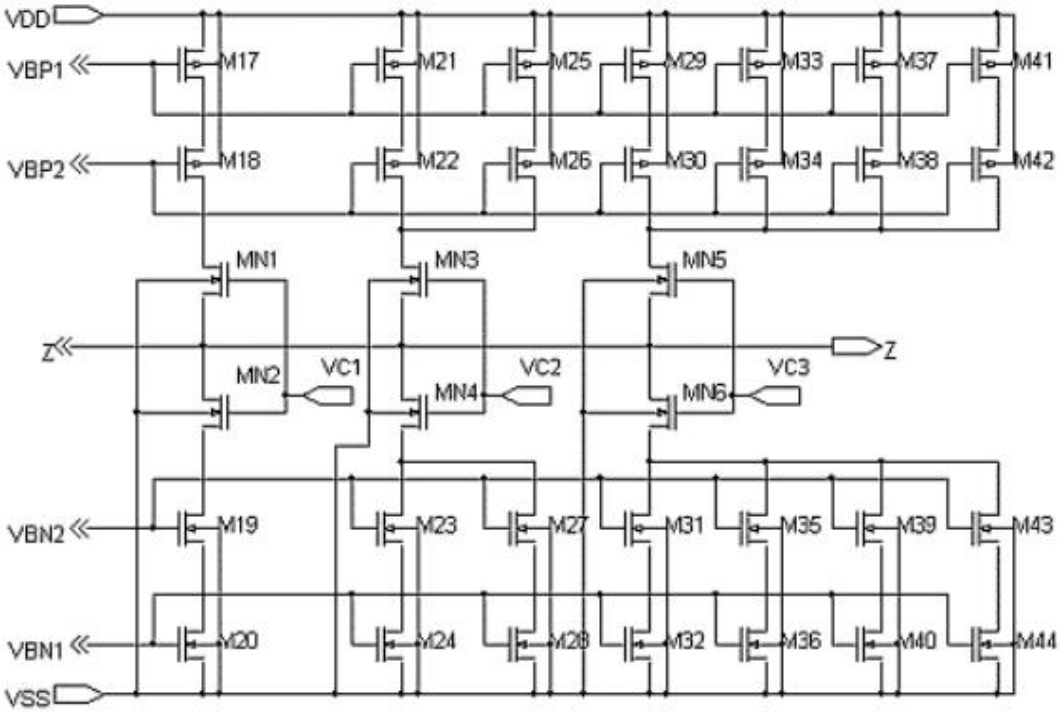

Figure 7. The output stage of the current conveyor that provides variable gain.

In Figure 7, transistors MN1-MN6 are NMOS transistors operating as switches. The control signals VC1-VC3 decide to add or not to add the branch currents to the output. Instead of using mirror transistors with current transfer ratio *m*, *m* transistors with equal geometry are paralleled in order to increase the current gain accuracy.

If a higher current gain is needed, paralleling more transistors with equal dimension will reduce the output impedance of the circuit. Therefore, adding parallel transistors in order to increase the current gain is valid up to a certain level. Instead, if the output stage in Figure-7 is connected to the output stage of the circuit given in Figure-8, then a current amplifier which can provide a total of 18dB gain in 6dB steps is obtained. The desired amount of gain can be provided by cascading the appropriate number of this circuit.

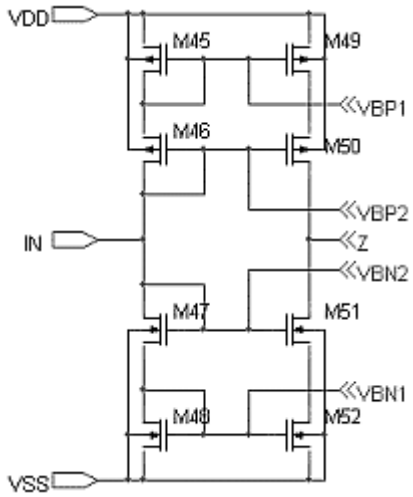

Figure 8. The input stage of the current amplifier.

4. SIMULATION RESULTS

AMS 0.35µ BSIM3v3 model parameters are used for PSPICE simulations. ±1.65V power supply is used during simulations. The aspect ratios of the transistors used in the CCII+ given in Figure 6 are tabulated in Table 2.

Table 2. The aspect ratios of the transistors used in Figure-6.

Device	W(u)/L(u)	Device	W(u)/L(u)
M1	11.75/2	M11	32/1.0
M2	50/2	M12	32/1.0
M3	50/2	M13	13.3/1.0
M4	11.75/2	M14	13.3/1.0
M5	1.5/1.0	M15	13.3/1.0
M6	1.5/1.0	M16	14.6/1.0
M7	1.5/1.0	M11c	24.7/0.3
M8	1.5/1.0	M12c	24.7/0.3
M9	6.25/1.0	M14c	3.4/0.3
M10	6.25/1.0	M15c	3.4/0.3

As high-Q discrete elements are not present in integrated RF receivers, the weak desired signal is down converted to baseband along with strong interferers. The linearity of the baseband circuits is therefore very important. If the input voltage range of the current conveyor used in the filter configurations of Section 2 is limited, then the linearity performance of the circuit will degrade due to clipping at the input and thus the dynamic range of the circuit will be decreased. For this reason a rail-to-rail input CCII should be used.

The DC voltage transfer characteristic of the current conveyor is obtained by sweeping the DC value of the power supply connected in y terminal and is given in Figure 9. As it is clear from Figure 9, the voltage at the x terminal follows the voltage at the y terminal in a wide input voltage range.

The frequency responses of the voltage and current gain of the current conveyor in Figure-6 are given in Figure 10 and Figure 11, respectively. The full simulation result of the baseband filter with variable gain that uses the current conveyor in Figure 6 is given in Figure 12.

The output current of the circuit is converted back to voltage by the total resistance value that provided the voltage-to-current conversion at the first stage in order to observe 6dB gain steps in full simulation. Thus variable gain can easily be seen as 6dB, 12dB and 18dB in Figure 12. The simulated power consumption of the proposed circuit is 5mW at maximum gain of 18dB.

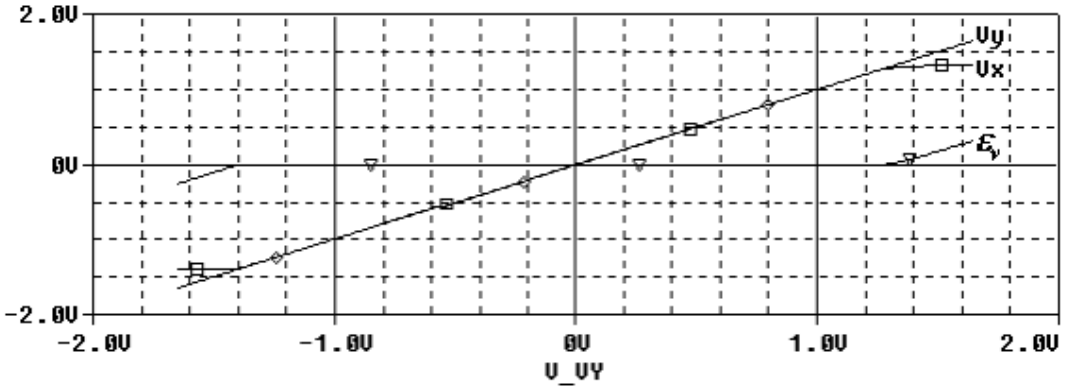

Figure 9. DC transfer characteristic of the current conveyor in Figure-6 with R_x=18.57kΩ.

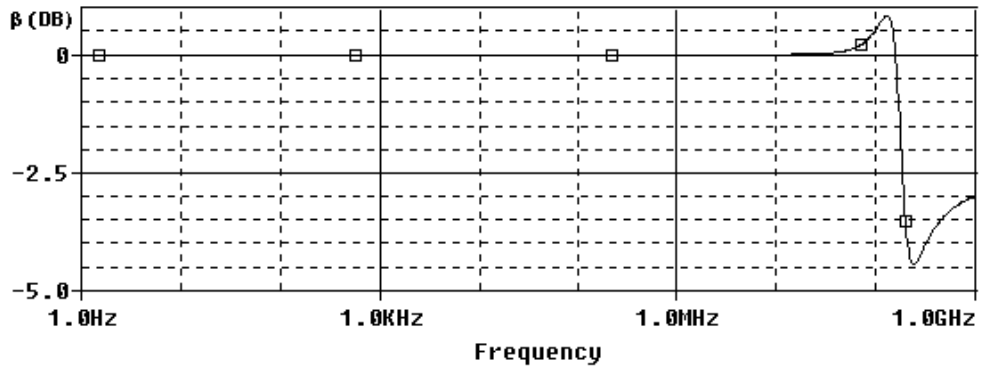

Figure 10. The frequency response of the voltage gain of current conveyor in Figure-6.

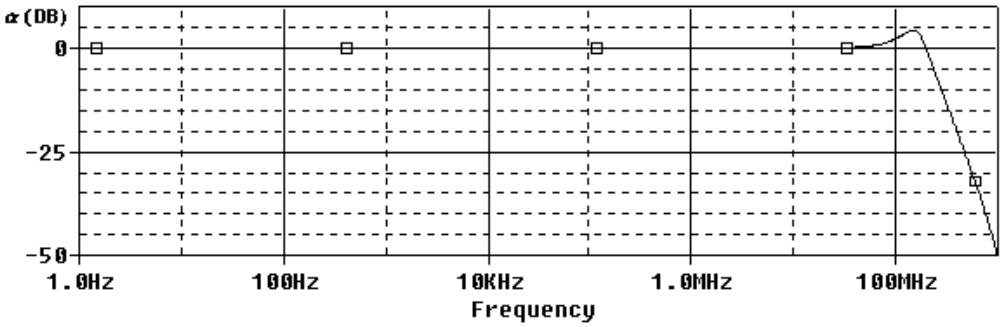

Figure 11. The frequency response of the current gain of current conveyor in Figure-6.

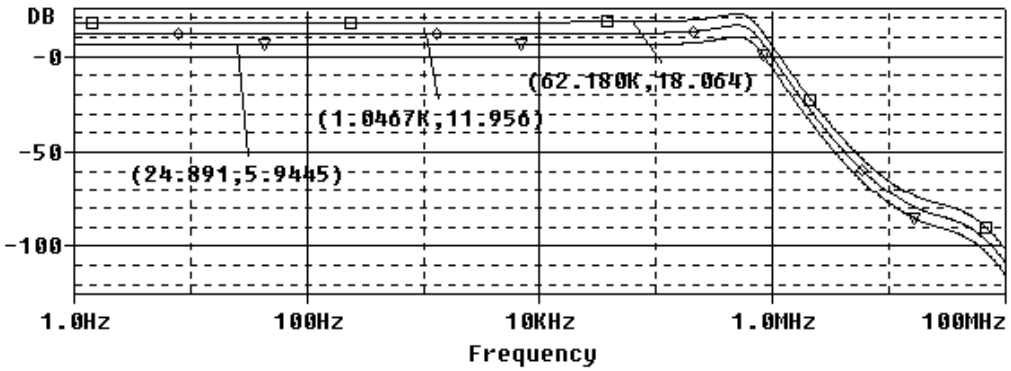

Figure 12. The frequency response of the baseband circuit with variable gain (with R_x=18.57kΩ).

5. CONCLUSION

In this study a part of the baseband stage of the on-chip modern radio receivers is designed in CM with low-voltage and low-power considerations. Besides the known advantages of CM operation to voltage-mode operation, the main advantage of this circuit is merging the voltage-to-current conversion and the variable gain at the first stage of the active filter. Therefore, both reduced die area and reduced power consumption can be obtained. If a higher order filter is required, then appropriate number of current-mode lowpass biquads can be connected in cascade to the transadmittance lowpass biquad that constitutes the first stage. In conclusion, the designed circuit is a fourth order lowpass filter with Chebyshev characteristic. Both active filters are designed as single amplifier biquads with low power and die area considerations.

All designed circuits are implemented in compliance with standard CMOS processes and the theoretical studies are validated by the simulation results obtained by computer-aided tools. If a further reduction in power consumption is required, then Class-AB current conveyor topologies that draw small bias currents may be used. However, such Class-AB CCII topologies either require twin-tub technology or unsuitable for low-voltage operation due to body effect. The future work may involve the investigation of low voltage low power rail-to-rail Class-AB CCII topologies that can be implemented in a standard n-well CMOS technology.

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