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A Lossless Simulated Floating Inductor Based on the Second-Generation Current Conveyors

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WHAT IS ALREADY KNOWN ON THIS TOPIC?

- *Passive inductors have some disadvantages in ICs, such as large area, high cost, low-quality factor, low inductance value, lack of tunability, etc.; thus, SFI circuits are preferred in ICs.*

WHAT DOES THIS STUDY ADD ON THIS TOPIC?

- *A lossless CCII-based SFI circuit is designed which acts as a floating passive inductor.*
- *The proposed SFI is available for ICs.*

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ABSTRACT

In this study, a new lossless simulated floating inductor (SFI) is proposed. The proposed circuit contains three non-inverting second-generation current conveyors. It consists of a capacitor and three resistors, but all the passive elements are floating. The proposed SFI requires one passive element matching condition. A second-order low-pass filter (LPF) is given as an application example. All the simulations are performed through the SPICE program. Also, some experiments for the proposed SFI and second-order LPF filter are conducted. All the simulations are performed by using the macro model of the AD844, and all experimental tests are achieved by using the AD844s.
Index Terms—AD844, second-generation current conveyors (CCII+), lossless, simulated floating inductor (SFI), synthetic inductor

I. INTRODUCTION

An inductor is a vital component for analog circuits. However, passive inductors have some disadvantages in integrated circuits (ICs), such as large area, high cost, low-quality factor, low inductance value, lack of tunability, etc. [1-6]. So, simulated inductors (SIs) are preferred in ICs. The SIs can be easily obtained by using active building blocks (ABBs) such as second-generation current conveyors (CCIIs), current feedback operational amplifiers (CFOAs), etc. The CCII is one of the most basic and preferred ABBs [4]. In the literature, many simulated floating inductors (SFIs) have been developed by using various ABBs such as ZC-VDCC [1], S-CCI [2], MO-DXCCTA [3], CCII [4], CCII and OTA [5], VCII [6], DVTC [7], VDTA [8], CBTA [9], VDBA [10], VDTA [11], CCTA [12], ZC-CFCCC [13], CFOA [14], DVCC and CCII [15], VCG-CCII [16], CCCII and OA [17], CCII and OTA [18, 19], CCII [20-22], INIC [23], CDBA [24], ICFOA [25], OTA and DVB [26], VDDDA [27], ECCII and DVB [28], LT1228 and OA [29], VCII [30], VDIBA [31], which have the following handicaps:

Some SFIs introduced in refs. [8, 10, 11, 23, 26, 28, 31] are lossy. A few structures in refs. [21, 30] have more than three resistors. Numerous circuits in refs. [4-6, 15, 17-20, 26, 28-30] have been designed with different types of active devices. The SFIs in refs. [2-9, 12, 13, 15-22, 25-28, 30] can be realized with more than three AD844s [32] /operational transconductance amplifiers/operational amplifiers/other commercially available active devices in addition to external resistors. A few designs given in refs. [17, 19] are temperature-dependent because they use bipolar junction transistors (BJTs). The proposed SFI is more efficient than the circuits specified in refs. [1-19, 25, 27-30] regarding the operating frequency range point of view. The SFIs in refs. [1-9, 11, 13-15, 18, 19, 20-22, 24, 26-28, 30] have a grounded capacitor. Further, many circuits in refs. [1, 3, 5-9, 11, 13, 15-19, 22-28] do not suffer from passive/active component matching conditions. Also, some simulated grounded inductors (SGIs) have been published in the literature [33-40] in which the SGIs in refs. [36, 37] are fractional-order. The previously published SFIs and the proposed one are comparatively shown in Table I. Acronyms for the various active devices in Table I are demonstrated in Table II.

TABLE I. COMPARISON TABLE FOR THE SIMULATED FLOATING INDUCTORS

References	Figure	# of ABBs	Lossless	# of R/C G(F)	Technology	Operating Frequency Range (Hz)	Supply Voltage (V)	Power Consumption (W)
[1]	3b	1 ZC-VDCC	Yes	0(0)/1(0)	0.18 µm	20 k-1.8 M	±0.9	0.326 m
[2]	3	1 S-CCI	Yes	1(1)/1(0)	0.18 µm	40 k-40 M	±1.5	6 m
[3]	2	2 MO-DXCCTA	Yes	0(0)/1(0)	0.18 µm	1 k-1 M	±1.25	2.96 m
[4]	3	1 DO-CCII, 2 CCII+	Yes	3(0)/1(0)	0.18 µm	100-3 M	±1.25	1.26 m
[5]	1	1 DO-CCII, 1 DO-OTA	Yes	0(1)/1(0)	0.18 µm	5-80 k	–	–
[6]	1	1 VCII±, 1 VCII+, 1 VCII–	Yes	0(0)/1(0)	0.18 µm	100 k-3 M	±0.9	1.92 m
[7]	7a	2 DVTC	Yes	0(2)/1(0)	0.25 µm	~60 k-60 M	±0.75	1.18 m
[8]	2a	2 VDTA	No	1(0)/1(0)	0.25 µm	~200 k-5 M	±1	2.4 m
[9]	4	2 CBTA	Yes	2(0)/1(0)	0.18 µm	~500-3 k	±0.9	–
[10]	2a	3 VDBA	No	0(0)/0(1)	0.25 µm	2 M-20 M	±0.75	1.13 m
[11]	3a	1 VDTA	No	1(0)/1(0)	0.25 µm	~2 M-50 M	±1	0.8 m
[12]	2	2 CCTA‡	Yes	0(1)/0(1)	0.09 µm	20 k-43 M	±1.2	4.5 m
[13]	3	2 ZC-CFCCC	Yes	0(0)/1(0)	0.18 µm	100-2.94 M	±2.5	4.94 m
[14]	6	3 CFOA	Yes	0(3)/1(0)	0.18 µm	100 k-10 M	±1.25	3.3 m
[15]	14	1 DVCC, 2 CCII+	Yes	1(1)/1(0)	0.25 µm	100 k-10 M	±1.5	–
[16]	12	2 VCG-CCII	Yes	0(2)/0(1)	0.35 µm	0.3-30 k	±1	1.4 m-6 m
[17]	1	1 DO-CCCII, 1 OA	Yes	0(0)/0(0)	BJTs, LF356	0.1-1 k	±2.5	–
[18]	1a	1 DO-CCII, 1 OTA	Yes	1(0)/1(0)	0.35 µm	800-45 M	±1.5	1 m
[19]	2	1 DO-CCCII, 1 OTA	Yes	0(0)/1(0)	BJTs	3 k-1 M	±2.5	–
[20]	5	2 CCII+, 1 DO-CCII	Yes	0(0)/1(0)	0.35 µm	–	±2.5	–
[20]	6	4 CCII–	Yes	0(0)/1(0)	0.35 µm	–	±2.5	–
[21]	2	6 CCII+	Yes	0(4)/1(0)	AD844	10n-10 k	–	–
[22]	1	5 CCII+	Yes	2(2)/1(0)	–	–	–	–
[23]	2	2 INIC	No	0(2)/0(1)	AD844	~10-1 M	±12	–
[24]	3	3 CDBA	Yes	*/1(0)	0.5 µm	–	±2.5	–
[24]	4	4 CDBA	Yes	*/1(0)	0.5 µm	–	±2.5	–
[25]	3	2 ICFOA	Yes	0(2)/0(1)	0.18 µm	200-5M	±1.25	1.49 m
[26]	1c	2 DO-OTA, 1 DVB	No	0(0)/1(0)	–	–	–	–
[27]	3	2 VDDDA	Yes	0(0)/1(0)	LM13700, AD830	3 k-1.56 M	±5	–
[28]	1	1 DVB, 2 ECCII+, 1 ECCII–	No	0(1)/1(0)	EL2082, AD830	~1 k-3 M	±5	–
[29]	3	2 LT1228, 1 OA	Yes	0(0)/0(0)	LT1228, LM741	~1 k-1 M	±5	0.128
[30]	3	2 VCII+, 2 VCII–	Yes	0(4)/1(0)	0.18 µm	200 k-1 M	±0.9	–
[31]	9	2 VDIBA	No	0(1)/0(1)	0.18 µm	~1 m-1 M	±1	–
Proposed SFI		**3 CCII+**	**Yes**	**0(3)/0(1)**	**AD844**	**10-1 M**	**±12**	**0.478**

*Use MOS transistors. ‡With 2SA721 and 2SC1327. –, not available.

TABLE II. ACRONYMS FOR THE VARIOUS ACTIVE DEVICES IN TABLE I

Acronyms	Active Elements
CCI	First-generation current conveyor
S-CCI	Subtractor connected first-generation current conveyor
CCII	Second-generation current conveyor
CCII+	Plus-type CCII
CCII–	Minus-type CCII
DO-CCII	Dual output CCII
VCG-CCII	Voltage and current gained CCII
OTA	Operational transconductance amplifier
DO-OTA	Dual output OTA
OA	Operational amplifier
CFOA	Current feedback OA
ICFOA	Inverting CFOA
CCTA	Current conveyor transconductance amplifier
MO-DXCCTA	Multiple output dual-X CCTA
INIC	Current inversion negative impedance convertor
ZC-VDCC	Z-Copy voltage differencing current conveyor
VCII	Second-generation voltage conveyor
VCII+	Plus-type VCII
VCII–	Minus-type VCII
DVTC	Differential voltage to current converter
VDTA	Voltage differencing transconductance amplifier
CBTA	Current buffered transconductance amplifier
VDBA	Voltage differencing buffered amplifier
ZC-CFCCC	Z-Copy current follower current controlled conveyor
DVCC	Differential voltage current conveyor
DVB	Differential voltage buffer
VDDDA	Voltage differencing differential difference amplifier
ECCII+	Electronically adjustable CCII+
ECCII–	Electronically adjustable CCII–
VDIBA	Voltage differencing inverted buffered amplifier

In this study, a new plus-type CCII (CCII+)-based SFI is proposed. The proposed SFI uses three CCII+s, three resistors, and a capacitor. However, the proposed SFI possesses floating passive elements and suffers from a matching condition. Also, the proposed circuit suffers from electronic tunability. To electronically adjust the proposed circuit, operational transconductance amplifiers (OTAs) can be used instead of the resistors of the proposed circuit [41]. A floating capacitor in ICs can be easily realized in today's technologies [42].

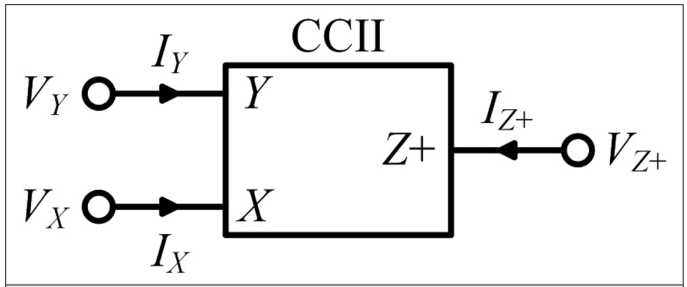

Fig. 1. Block diagram of the non-inverting second-generation current conveyors.

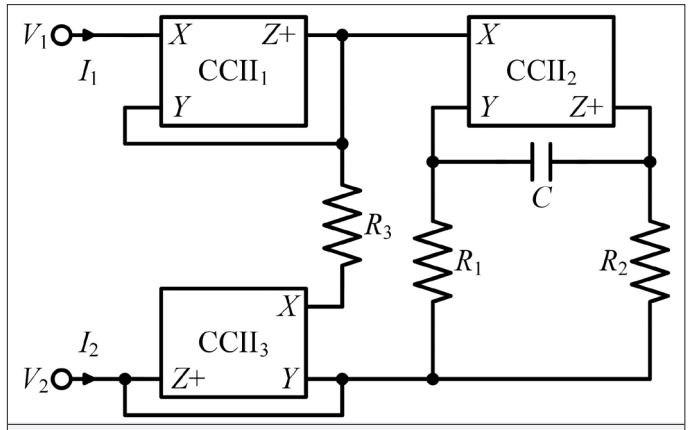

Fig. 2. The proposed simulated floating inductor.

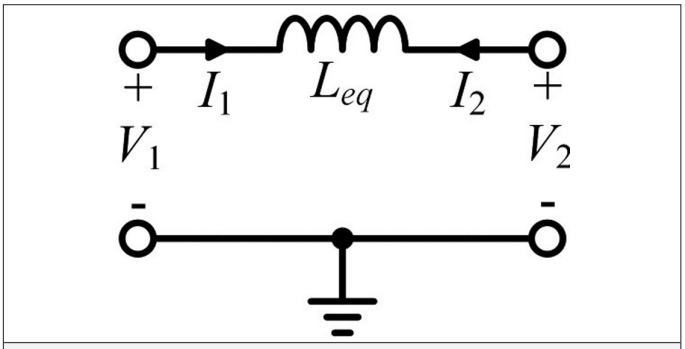

Fig. 3. Equivalent circuit for the proposed simulated floating inductor.

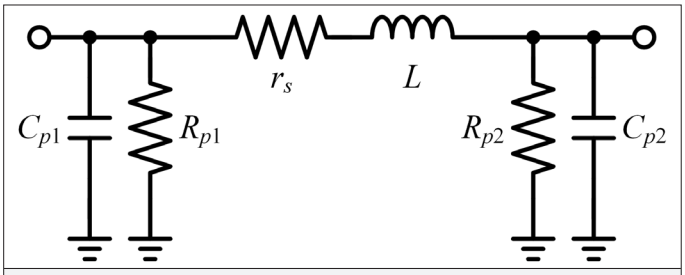

Fig. 4. Non-ideal equivalent circuit for the proposed simulated floating inductor.

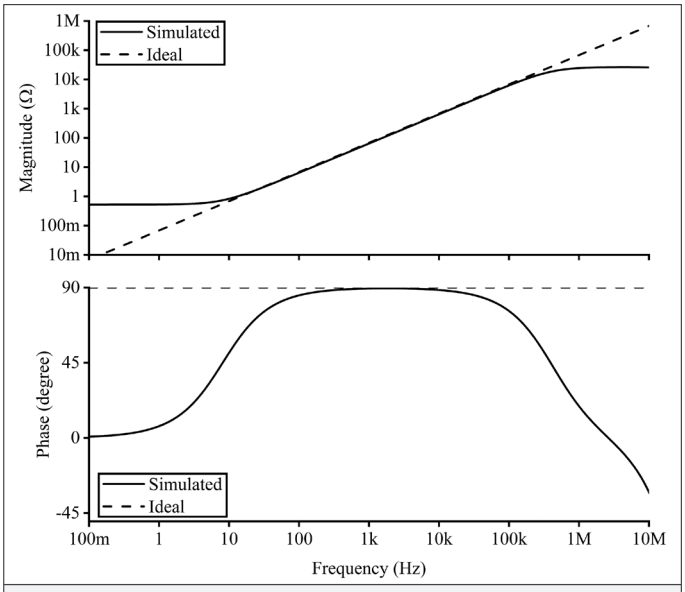

Fig. 5. AC results for the proposed simulated floating inductor.

The non-ideality analysis of the proposed circuit is performed. Moreover, a second-order low-pass filter (LPF) application is given. The simulations and experiments of the proposed SFI and application are performed by replacing the CCII+s with AD844s.

This paper is categorized as follows: the proposed SFI is introduced in Section II. The simulation results are shown in Section III. In addition, the second-order LPF application is given in Section IV. In Section V, some experiments are described. Finally, the paper concludes in Section VI.

II. THE PROPOSED SIMULATED FLOATING INDUCTOR

Theoretical relations among terminals of the CCII+ are given as a matrix equation in (1), and the symbol of this ABB is shown in Fig. 1.

$$\begin{bmatrix} I_Y \\ V_X \\ I_{Z+} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ \beta & 0 \\ 0 & \alpha \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \end{bmatrix} \tag{1}$$

Here, β and α are ideally equal to unity, and both are non-ideal gains. The proposed SFI circuit is demonstrated in Fig. 2. In Fig. 3, the equivalent circuit is also given. If $R_3 = R_1 \| R_2$ is chosen, the following admittance equation is ideally obtained:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{1}{sCR_1R_2} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \frac{1}{sL_{eq}} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2}$$

where $L_{eq} = CR_1R_2$. If β and α of the CCII+s in Fig. 2 with $R_3 = R_1 \| R_2$ are considered, the admittance equation is computed as below.

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{(\beta_1\beta_2)^{-1}}{sCR_1R_2} \begin{bmatrix} \dfrac{1+a(1-\alpha_2\beta_2)}{\alpha_1\alpha_2} & -\dfrac{1+a(1-\alpha_2\beta_3)}{\alpha_1\alpha_2(\beta_1\beta_2)^{-1}} \\ -\left(1+a(1-\alpha_3\beta_2)\right) & \dfrac{1+a(1-\alpha_3\beta_3)}{(\beta_1\beta_2)^{-1}} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{3}$$

where the term "a" is defined as

$$a = sC(R_1 + R_2) \tag{4}$$

Similarly, if $R_3 = R_1 \| R_2$ is not considered, the following admittance equation is found by

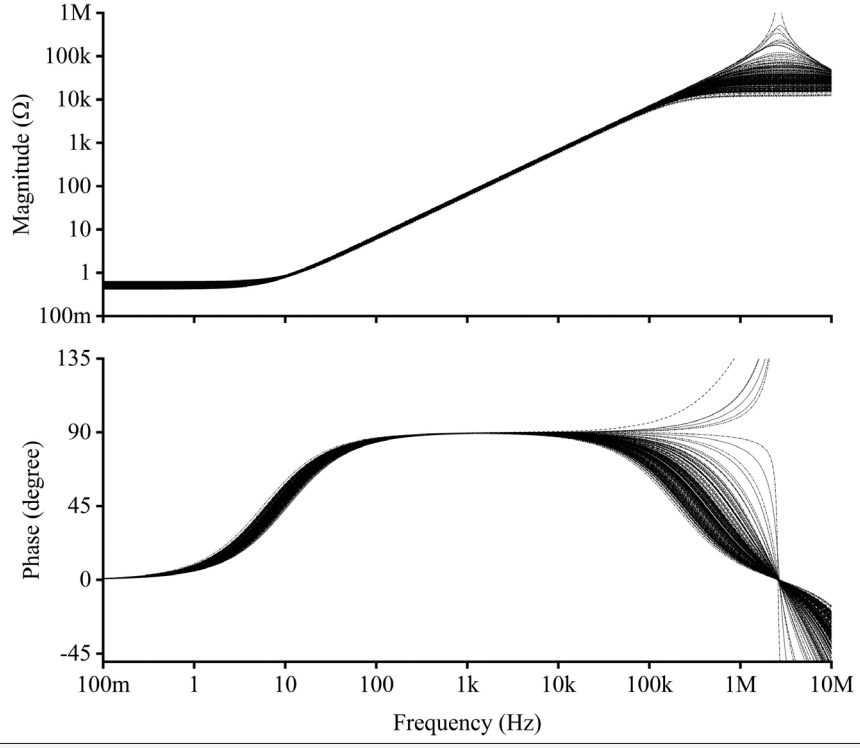

Fig. 6. Monte Carlo simulation results.

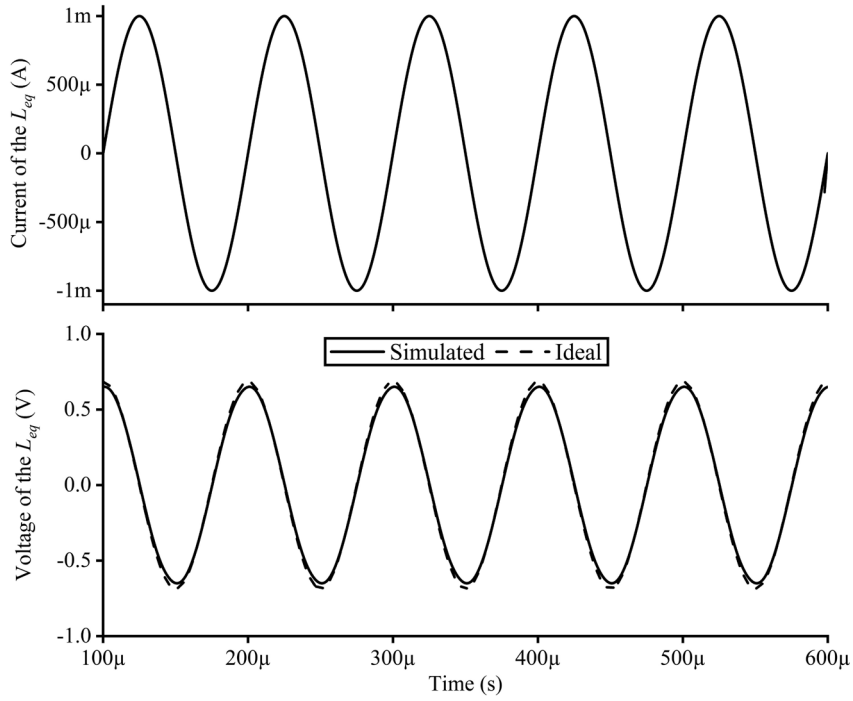

Fig. 7. Time domain simulation results.

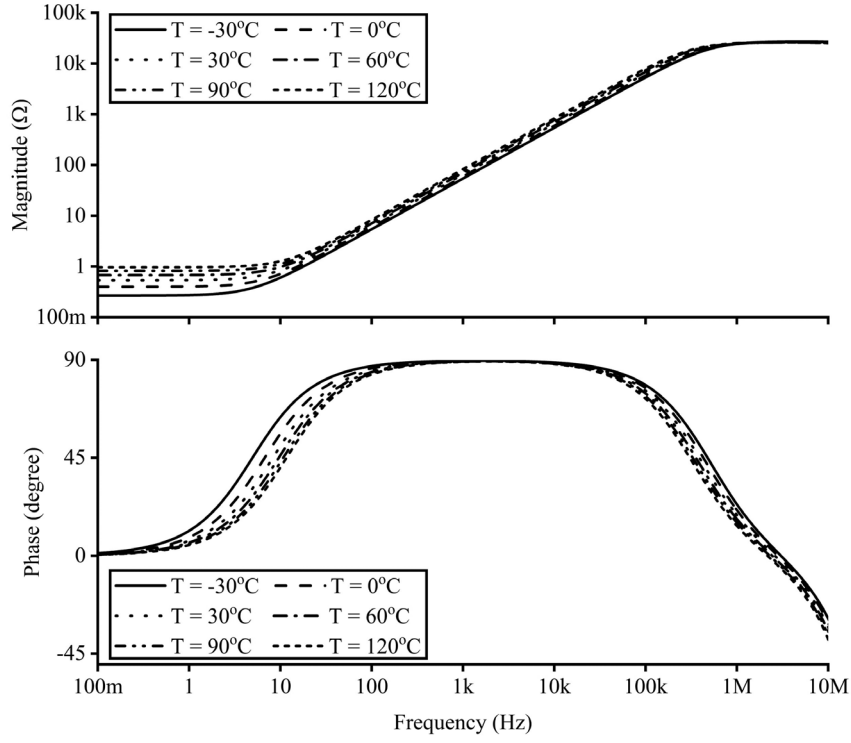

Fig. 8. Temperature simulation for the proposed simulated floating inductor.

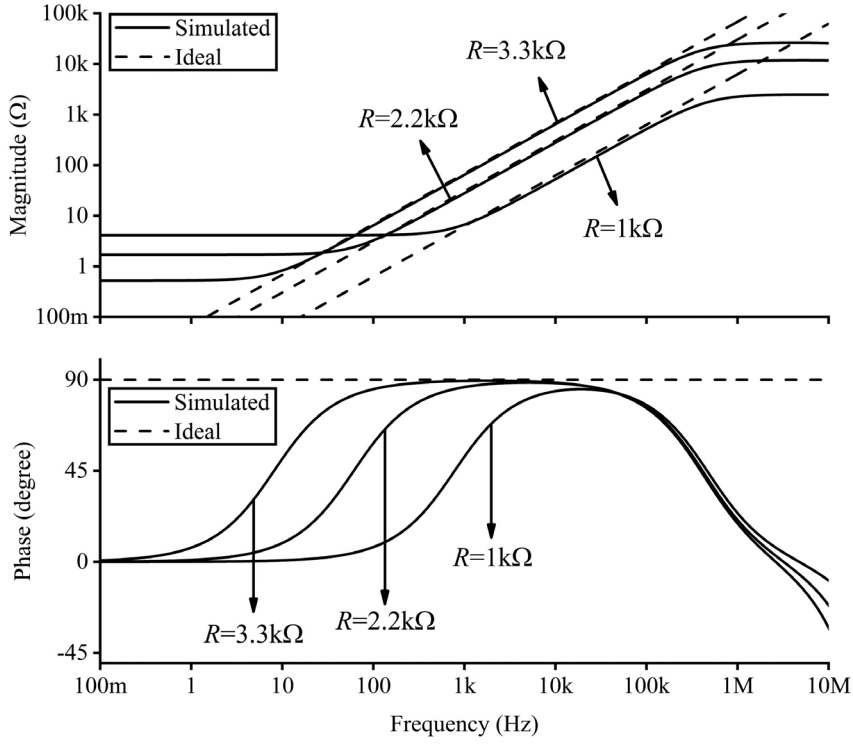

Fig. 9. AC results for different values of the resistors for the proposed simulated floating inductor.

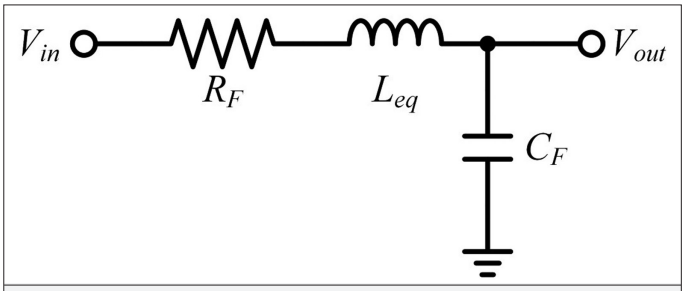

Fig. 10. Second-order low-pass filter as an example.

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{(\beta_1\beta_2)^{-1}}{sCR_1R_2R_3} \begin{bmatrix} \dfrac{b - sCR_1R_2\alpha_2\beta_2}{\alpha_1\alpha_2} & -\dfrac{b - sCR_1R_2\alpha_2\beta_3}{\alpha_1\alpha_2(\beta_1\beta_2)^{-1}} \\ -(b - sCR_1R_2\alpha_3\beta_2) & \dfrac{b - sCR_1R_2\alpha_3\beta_3}{(\beta_1\beta_2)^{-1}} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (5)$$

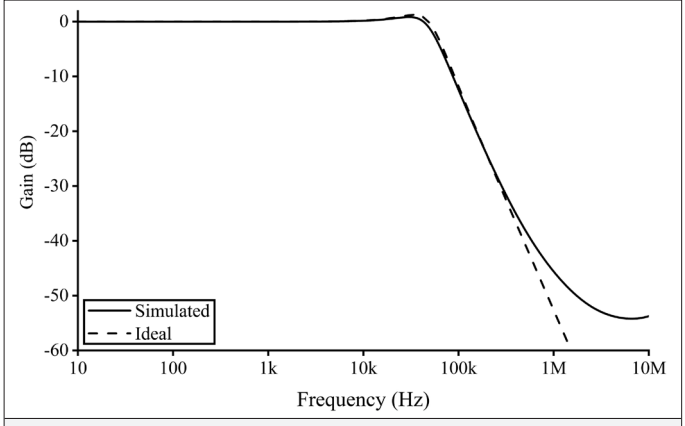

Fig. 11. Gain responses for the low-pass filter

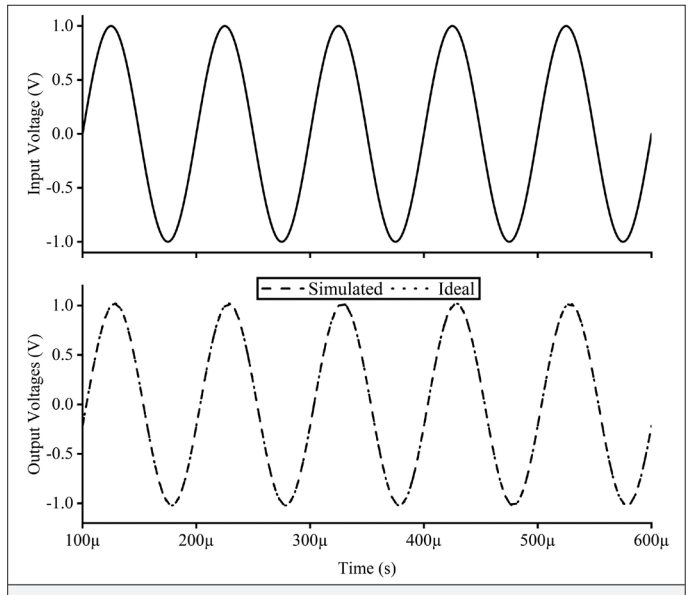

Fig. 12. Time-domain simulation results of the low-pass filter

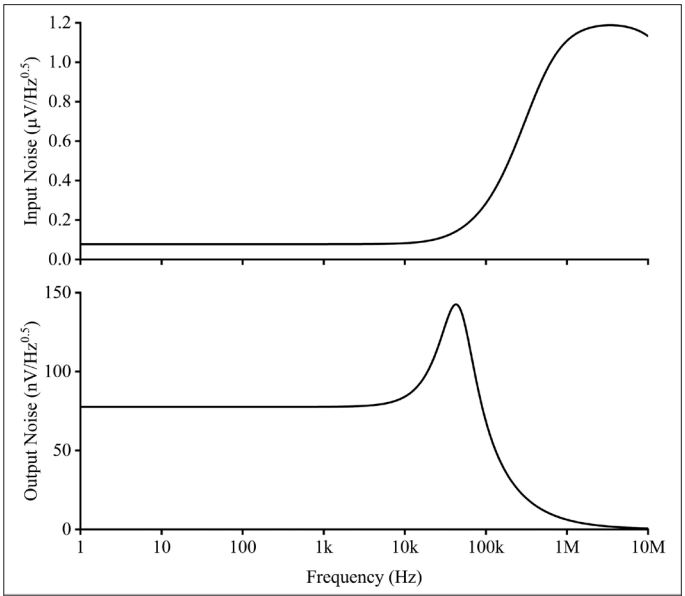

Fig. 13. Noise simulation results for the low-pass filter.

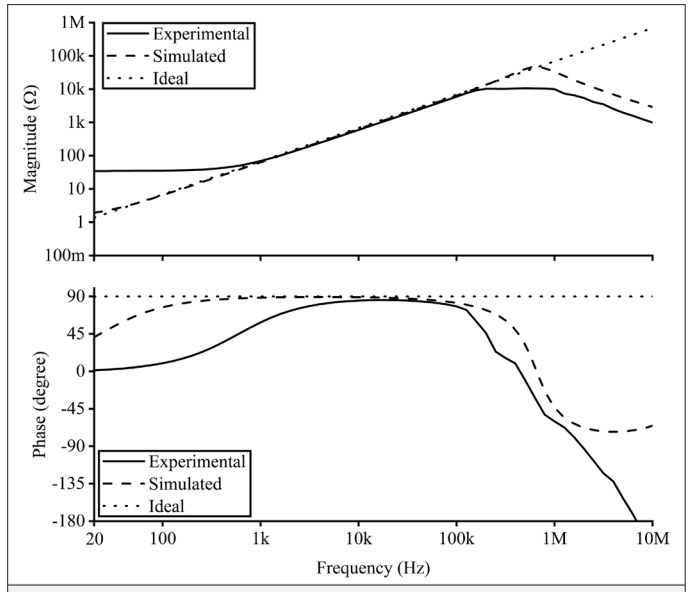

Fig. 15. AC analysis results for the simulated grounded inductor.

where the term *b* is defined as

$$b = R_3(1 + sC(R_1 + R_2)) \quad (6)$$

III. SIMULATION RESULTS

One CCII+ can be obtained from one AD844. Therefore, three AD844s are utilized in all the simulations. SPICE parameters of AD844 are received from the Analog Devices website [43]. Through the SPICE program, all the simulations are performed. ±12 V is applied as the DC supply voltages of the AD844s. The passive elements, C, R_1, R_2, and R_3 are, respectively, selected as 1 nF, 3.3 kΩ, 3.3 kΩ, and 1.65 kΩ. Thus, the equivalent inductor, L_{eq}, is ideally obtained as 10.89 mH according to (2). The non-ideal equivalent circuit of the proposed SFI is given in Fig. 4. According to the simulation results, $L \cong 10.27$ mH, $r_s \cong 1.43$ Ω, $R_{p1} \cong 26.3$ kΩ, $R_{p2} \cong 27$ kΩ, $C_{p1} \cong 840$ fF, and $C_{p2} \cong 3.62$ pF are found. In Fig. 5, AC results for the proposed SFI are comparatively plotted. As seen from Fig. 5, the proposed SFI works from about 10 Hz to 1 MHz. The Monte Carlo (MC) simulation of the SFI is presented in Fig. 6, in which the uniform deviation of all the passive components is 5%, and 200 samples are taken. The proposed SFI is much affected by random changes of the passive components at high frequencies, according to MC analysis results. Also, the output voltages of the proposed circuit are indicated in Fig. 7, where a sinusoidal input current with 1 mA peak at 10 kHz is applied. As seen from Fig. 7, the phase difference between current and voltage of the proposed SFI is 90.88°, which is very closed to 90°.

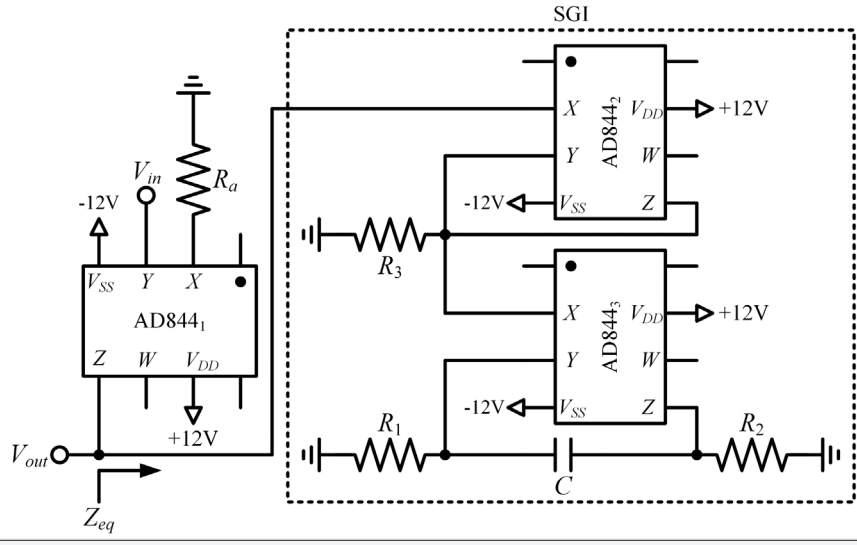

Fig. 14. Experimental circuit for the simulated grounded inductor

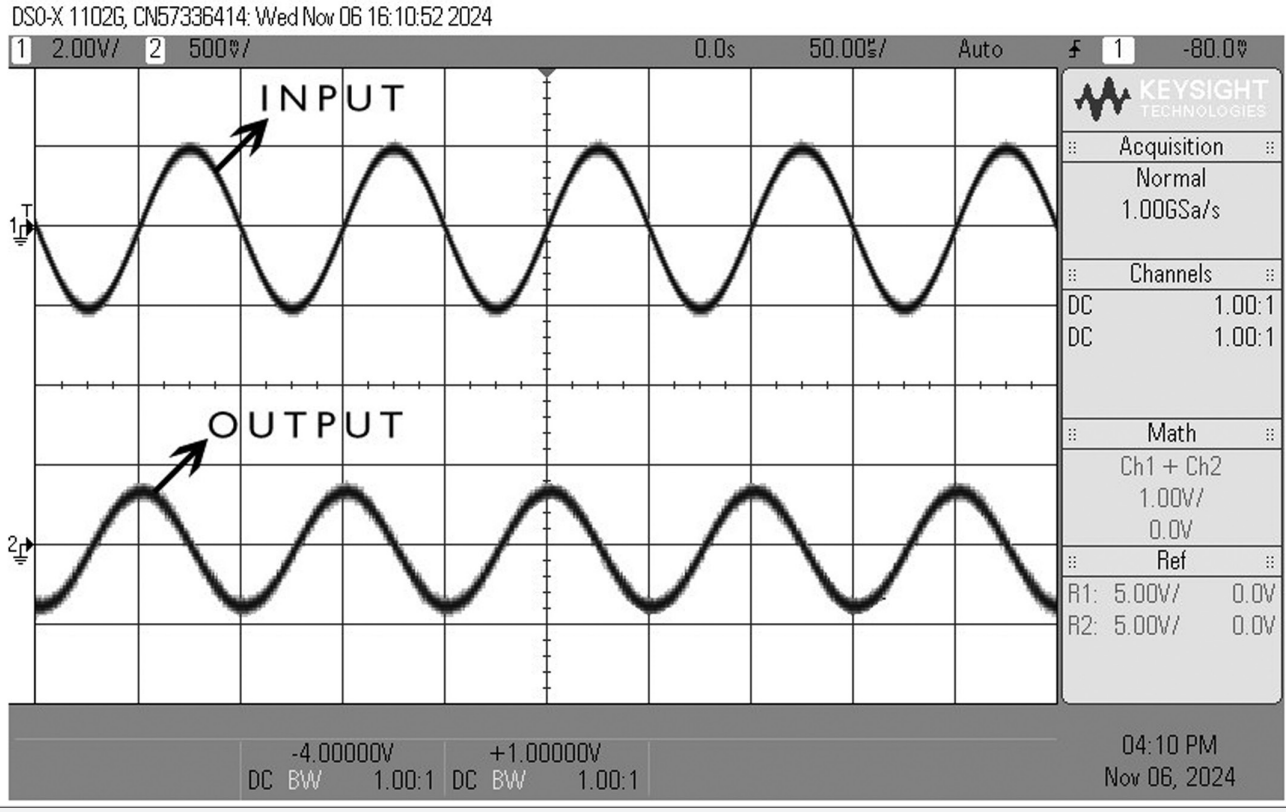

Fig. 16. Time-domain simulation for the simulated grounded inductor.

The temperature simulation is made, and the result is given in Fig. 8, in which the temperature values vary from −30°C to 120°C. The uniform deviation is selected as 5% for all the passive components in the temperature analysis. Besides, the linear temperature change of all the resistors for 1°C is taken as 15 ppm. According to the temperature analysis results, the temperature changes of passive components and the CCIIs have slight effects on the proposed SFI. In Fig. 9, AC results are plotted for different resistor values. In this simulation, the values of the resistors R_1 and R_2 respectively vary from 1 kΩ, 2.2 kΩ, and 3.3 kΩ, where R_3 is taken as $R/2$.

IV. AN EXAMPLE: SECOND-ORDER LOW-PASS FILTER

The second-order LPF example is expressed in Fig. 10. The proposed SFI given in Fig. 2 is used in the LPF in Fig. 10 as an inductor. The transfer function of the second-order LPF is depicted below.

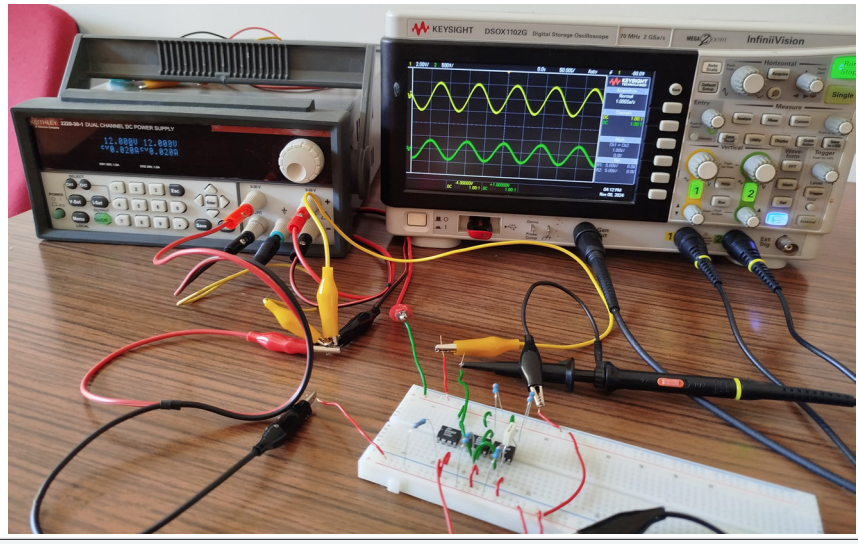

Fig. 17. The laboratory set-up realization for the simulated grounded inductor.

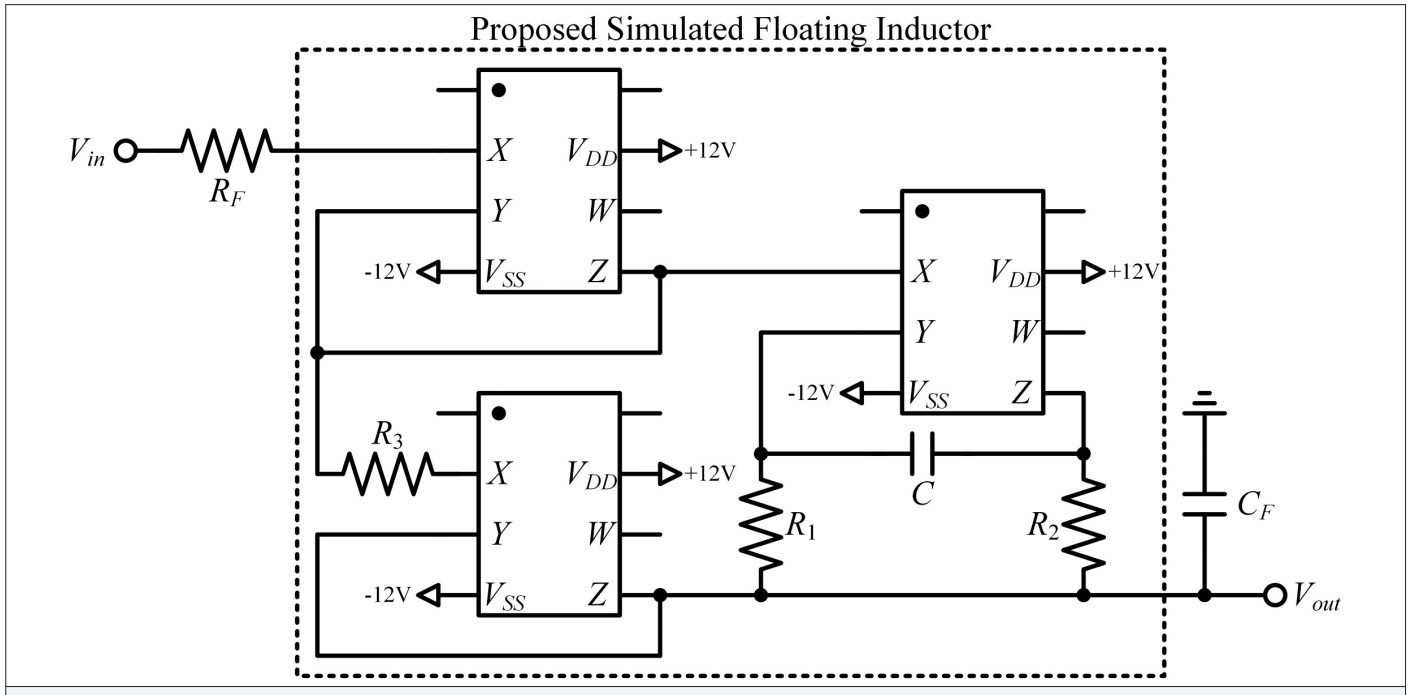

Fig. 18. Experimental circuit for the second-order low-pass filter shown in Fig. 11.

$$H(s)=\frac{1/\left(C_F L_{eq}\right)}{s^2+s\left(R_F/L_{eq}\right)+1/\left(C_F L_{eq}\right)}=\frac{1/\left(C_F C R_1 R_2\right)}{s^2+s\left(R_F/\left(C R_1 R_2\right)\right)+1/\left(C_F C R_1 R_2\right)} \quad (7)$$

From (7), the resonance frequency (f_0) is calculated as:

$$f_0=\frac{1}{2\pi}\frac{1}{\sqrt{C_F L_{eq}}}=\frac{1}{2\pi}\frac{1}{\sqrt{C_F C R_1 R_2}} \quad (8)$$

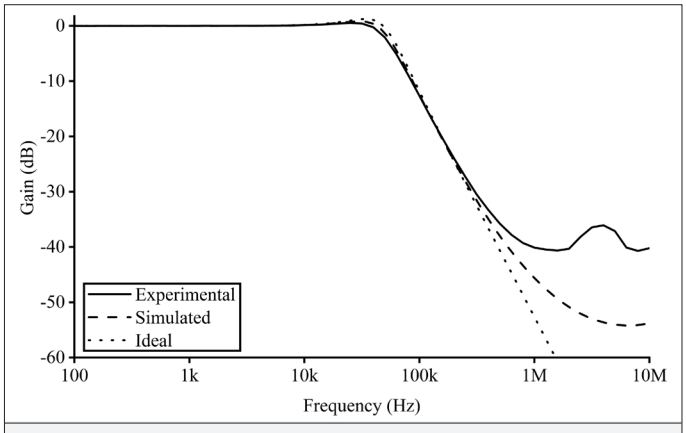

Fig. 19. AC analysis results for the second-order low-pass filter.

Quality factor (Q) is evaluated below.

$$Q=\frac{1}{R_F}\sqrt{\frac{L_{eq}}{C_F}}=\frac{1}{R_F}\sqrt{\frac{C R_1 R_2}{C_F}} \quad (9)$$

Simulations of the second-order LPF are made through the SPICE program. The value of the L_{eq} is obtained as 10.89 mH in which $C=1$ nF, $R_1=R_2=3.3$ kΩ, and $R_3=1.65$ kΩ are taken. In addition, R_F and C_F are chosen as 3.3 kΩ and 1 nF. As a result of selecting these values, f_0 and Q are, respectively, calculated as 48.2 kHz and 1. AC LPF results versus frequency and time domain simulation of the LPF results are, respectively, given in Figs. 11 and 12. It is seen from these figures that there is little difference between simulated and ideal results, which stems from the non-idealities of the AD844s. In Fig. 13, noise simulation results for the LPF are shown.

V. EXPERIMENTAL TESTS

In the experiments, the proposed SFI is tested by grounding the second port of the proposed SFI; thus, a SGI in Fig. 14 is obtained. There is no need to use the third CCII+ in the proposed SFI. AD844, known as the discrete IC component of the CCII, is used in the experiments. There is a parasitic resistor known as R_X connected in series with the X terminal of the AD844, and the value of R_X is 50 Ω. Also, there are a parasitic resistor and a capacitor known as R_Z and C_Z, respectively, connected in parallel to the Z terminal of AD844. The value of R_Z is 3 MΩ, while C_Z is 4.5 pF. An extra AD844 and an extra resistor ($R_a=3.3$ kΩ) are utilized as a current generator plotted in Fig. 14, where all the passive components are selected as $C=1$ nF, $R_1=R_2=3.3$ kΩ, and $R_3=1.65$ kΩ. ±12 V is applied as the

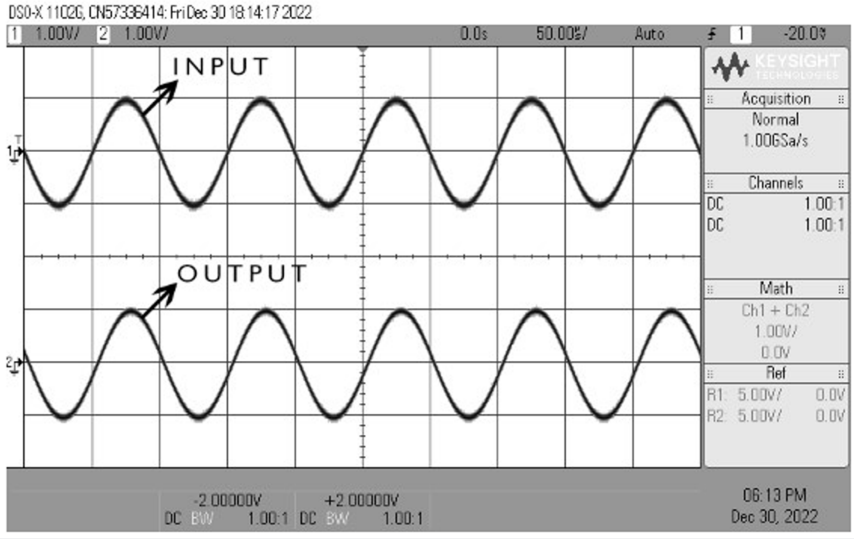

Fig. 20. Time domain simulation for the second-order low-pass filter.

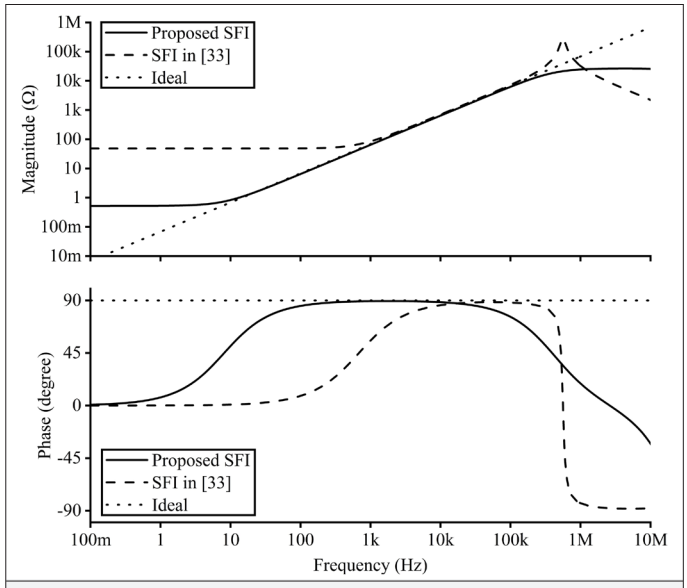

Fig. 21. The simulation results for the proposed simulated grounded inductorand the one in ref. [33].

DC supply voltage of the AD844s. AC analysis results for the SGI are indicated in Fig. 15, in which the experimental, simulated, and ideal responses are comparatively given. Further, $Z_{eq} = V_{out} \times Ra/V_{in}$ is taken. When performing AC analysis, a 4 V peak-to-peak magnitude voltage signal is applied as input to the circuit. The differences among the experimental, simulation, and ideal results are due to the parasitic impedances of the AD844s, the breadboard used, and the tolerance of the resistors. In Fig. 16, the input and obtained output voltages are indicated in the time domain, where a sinusoidal voltage with 4 V peak-to-peak magnitude is applied to V_{in} and the frequency of this signal is 10 kHz. Also, the laboratory set-up realization of the circuit in Fig. 14 is given in Fig. 17.

The second-order LPF given in Fig. 10 is also tested in the experiments. The experimental circuit for this filter is shown in Fig. 18. In this experiment, all the resistors except R_3 (R_1, R_2, R_F) are taken as 3.3 kΩ, while R_3 is chosen as 1.65 kΩ. Both capacitors are selected as 1 nF. Thus, f_0 and Q of the LPF are ideally calculated as 48.2 kHz and 1, respectively. AC analysis and time domain simulation results are given in Figs. 19 and 20, respectively. A sinusoidal voltage with 2 V peak-to-peak magnitude is applied to V_{in} and the frequency of this signal at 10 kHz in the time domain simulation is given in Fig. 20.

The proposed SFI is compared with the SFI in [33] where $R_1 = R_2 = 3.3$ kΩ and $C = 1$ nF are taken for both SFIs. Also, $R_3 = 1.65$ kΩ is chosen for the proposed one. Thus, $L_{eq} = 10.89$ mH is evaluated. The simulation results are comparatively shown in Fig. 21.

VI. CONCLUSION

A new SFI based on the positive-type CCII is proposed. This SFI circuit includes three CCII+s, three resistors, and a capacitor. The proposed circuit is lossless. Further, the proposed circuit is minimally affected by temperature changes. As can be seen from the MC analysis results, the random changes of the passive components have a significant effect on the proposed circuit at high frequencies. Nevertheless, all the passive components are floating, and the proposed circuit suffers from a passive component matching condition. It is tested in a second-order LPF application circuit. AD844s are used instead of the CCII+s in the simulations and experiments. Simulations are performed through the SPICE program. Additionally, the experiments are built on a breadboard. The proposed circuit is transformed into the SGI circuit so that the experiments of the proposed SFI can be carried out. Also, a Keitley DSOX1102G as a digital oscilloscope and a Keitley 2220-30-1 as a DC power supply are used in the experiments. It is observed from the simulation results that the proposed SFI works from about 10 Hz to 1 MHz. However, there is a bit of difference caused by the parasitic impedances of the breadboard and the non-idealities of the AD844s.

Availability of Data and Materials: The data that support the findings of this study are available on request from the corresponding author.

Peer-review: Externally peer-reviewed.

Author Contributions: Concept – T.Y., E.Y.; Design – T.Y., E.Y.; Supervision – T.Y., E.Y.; Materials – T.Y., E.Y.; Data Collection and/or Processing – T.Y., E.Y.; Analysis and/or Interpretation – T.Y., E.Y.; Literature Review – T.Y., E.Y.; Writing – T.Y., E.Y.; Critical Review – T.Y., E.Y.

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